FURUNO

FURUNO GNSS Receiver

GT-100

Hardware Specifications

(Document No. SE22-410-003-02)

FURUNO ELECTRIC CO., LTD.

www.furuno.com

IMPORTANT NOTICE

Any information of this documentation shall not be disclosed to any third party without permission of the publisher, FURUNO ELECTRIC CO., LTD.

FURUNO ELECTRIC CO., LTD. reserves the right to make changes to its products and specifications without notice.

All brand and product names are registered trademarks, trademarks or service marks of their respective holders.

The following satellite systems are operated and controlled by the authorities of each government.

- GPS, SBAS(WAAS): USA
- GLONASS: Russia
- Galileo, SBAS(EGNOS): Europe
- QZSS, SBAS(MSAS): Japan
- NavIC, SBAS(GAGAN): India
- BeiDou: China

Thus FURUNO is not liable for the degradation of the above systems so therefore FURUNO cannot guarantee specification based on their conditions. User is expected to be familiar with the System and make full use of it with their own responsibility.

We pay through attention about the software of this product. But, if perchance you found a bug or a trouble, please feel free to contact us directly. We will check it, and if it is a bug, we may send you a new version with a bug fix. If perchance we found a bug or a trouble, we may send you a new version after we contact you.

When we send you the new version software, we may ask you to update software. Therefore, we strongly recommended being able to access to serial port of this product from outside of your product to make software update easy. In addition, we also strongly recommend connecting between serial port of this product and network to remote access and update software.

This product must not be used for military and/or antisocial purposes such as terrorism, and shall not be supplied to any party Intending to use the products for such purposes.

This product has been designed for consumer equipment and devices. This product is not intended for use in, and must not be used for, any application of nuclear equipment, driving control equipment for aerospace or any other unauthorized use. With the exception of the above-mentioned banned applications, for applications involving highs of safety and liability such as medical equipment, burglar alarm equipment, disaster prevention equipment and undersea equipment, please contact an FURUNO sales representative and/or evaluate the total system on the applicability. Also, implement a fail-safe design, protection circuit, redundant circuit, malfunction protection and/or fire protection into the complete system for safety and reliability of the total system.

Revision History

Version	Changed contents	Date
0	Initial release	2022.06.22
1	Change the figure in section 4.1 Correct items in Table 4.2 Add items in Table 5.1 Add items in Table 5.2 Add section 5.4 Change the contents in section 5.5 Add items in Table 5.6.2 Change the figures in section 7.1 Add a note in section 7.1 Correct the weight in section 7.2 Add the storage conditions in section 8.3 Change the figure in section 8.4 Change the figure in section 8.5 Change the figure in section 8.6 Add the marking specifications in chapter 9	2022.12.19
2	IMPORTANT NOTICE Change the figure in section 3 Change the contents in Table 4.2 Change the contents in Table 5.6.1 Change the contents in Table 5.6.2	2023.05.12

Table of Contents

1 Outline

This document contains the specification pertinent to the GNSS module.

2 Features

2.1 Product Overview

GT-100 is Dual band, multi constellation GNSS receivers.
◆ GT-100 support L1 Band and L5 Band.
◆ GT-100 support GPS, GLONASS, BeiDou, Galileo, NavIC, SBAS and QZSS as multi constellation.

GT-100 output accurate time information.
◆ GT-100 support PPS (Pulse per Second) output synchronized with UTC time or GPS time and frequency output that can be set arbitrarily.

The products support the debug feature for GNSS application.
◆ Internal Antenna Diagnostic function.

The products include an embedded NVM for firmware updates.
◆ Size: 16Mbit
◆ Memory Structure: STT-MRAM

The products have an UART interface. And the following message format is supported.
◆ NMEA Message

Table 2.1 General Specifications[1)]

Items	Description		Notes
GNSS reception capability	GPS L1C/A	L1	32 channels
	GLONASS L1OF	L1	
	Galileo E1	L1	
	Beidou B1I	L1	
	Beidou B1C	L1	
	QZSS L1C/A	L1	
	SBAS L1	L1	
	NavIC L5	L5	
	GPS L5	L5	30 channels
	Galileo E5a	L5	
	Beidou B2a	L5	
	QZSS L5	L5	
Environment Robustness	Anti-Jamming	●	-
	Anti-Spoofing	●	-
	Multipath mitigation	●	-
	T-RAIM	●	-
	Antenna current detection	●	-
Serial data format	NMEA[2)]	●	Default 115200bps
Antenna	Active antenna	●	
	Passive antenna	●	External LNA required.
Operational limits	Altitude	18,300m	Based on Wassenaar arrangement specification
	Velocity	515 m/s	

Notes:
1) See the function specifications for details.
2) See the protocol specifications for details.

3 Functional Overview

The internal key device for GT-100 is *eRide*OPUS 9. The latest Furuno monolithic GNSS receiver chip with an ARM-Cortex processor (for signal tracking and processing), PLL synthesizer, Down-converter, ADC, DSP and STT-MRAM (for firmware and data storage).

GT-100 also include a TCXO (for reference clock), RTC (for real-time clock) 32 kHz crystal, SAW filter, and antenna current detection circuit. The block diagram is shown in Figure 3.1.

GT-100 have a built-in function (FGEN) for generating high-precision clock pulses in the GNSS receiver chip. GT-100 output a PPS signal or a clock pulse of any frequency from its OCLK0, OCLK1 and OCLK2. The GT-100 have an input pin, ICLK, to allow time synchronization with an external PPS or clock. Refer to the function specifications and protocol specifications for usage.

RF_IN is the signal line on which the GNSS signal input and the bias voltage for antenna power supply are superimposed. By applying a voltage to VCC_ANT, the bias voltage is superimposed on RF_IN. The antenna current detection circuit detects whether the current flowing from VCC_ANT to RF_IN is insufficient or excessive. This status can be known by serial communication.

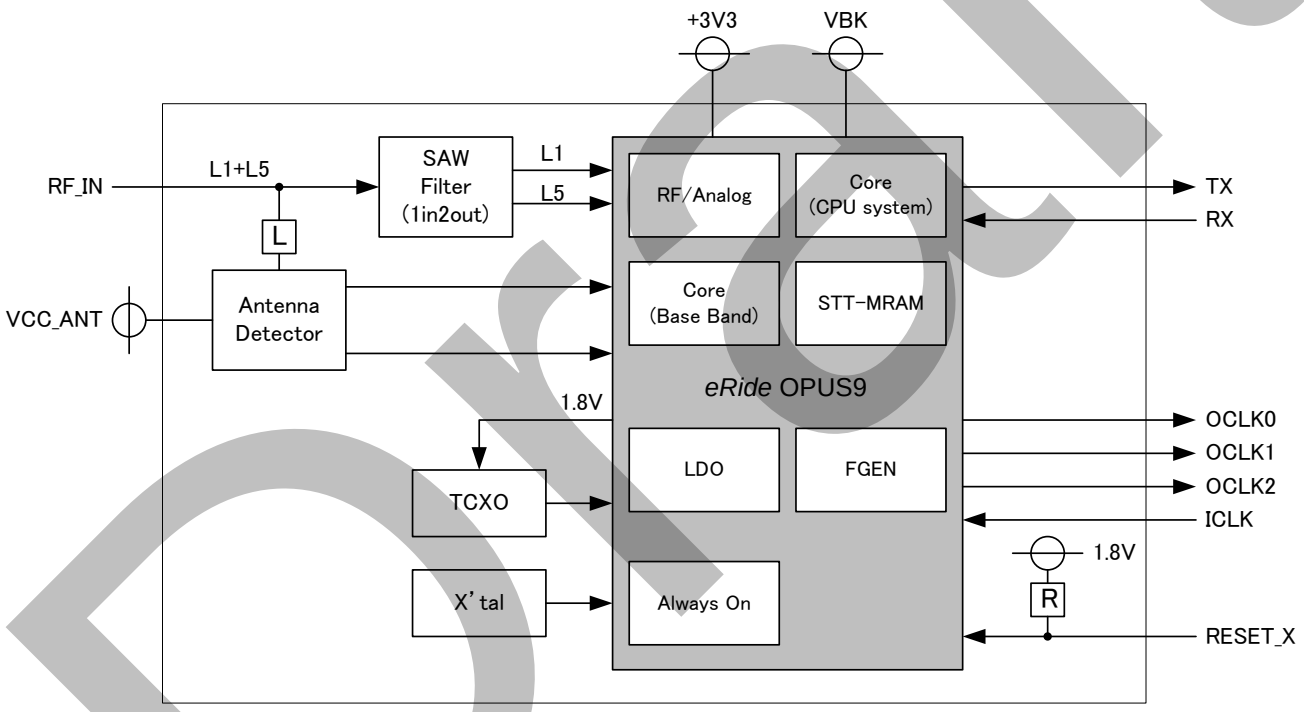
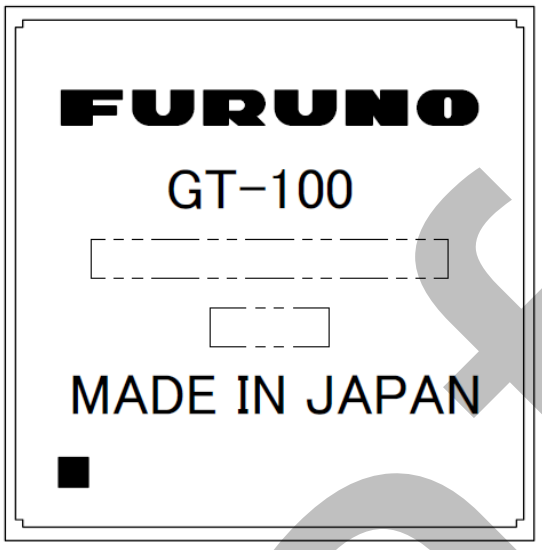


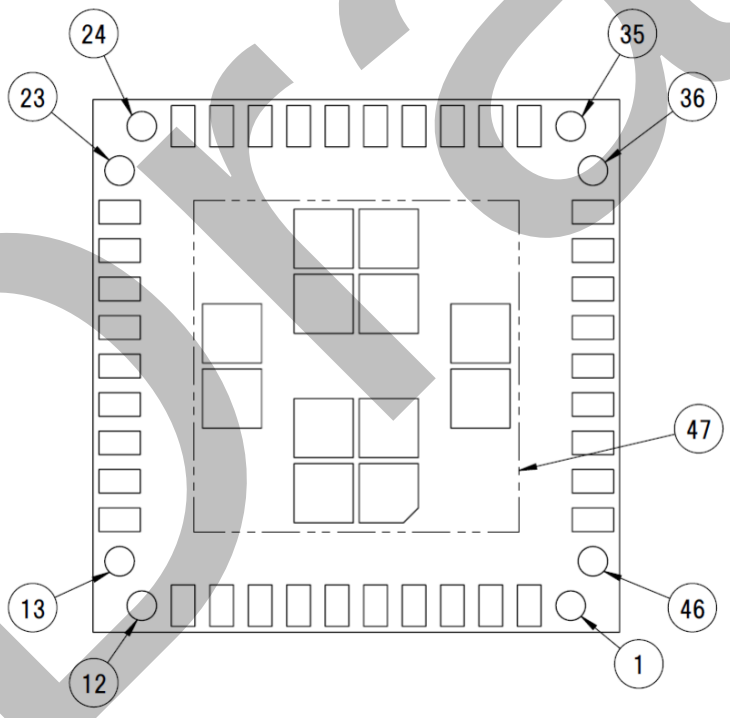
Figure 3.1 Block Diagram

4 I/O Signal Description

4.1 Pin Layout



TOP View



BOTTOM view

Note: GND pads of the center are put together as Pin No.47.

4.2 GT-100 Signal Description

Table 4.2 I/O Signal Description

#	GT-100 Pin Name	I/O	I/O Voltage	PU/PD[1)]	Reset State	Unused	Description
1	NC	-	-	-	-	OPEN	-
2	GND	-	-	-	-	-	-
3	RESERVE	-	-	-	-	OPEN	Don't connect to GND.
4	RESERVE	-	-	-	-	OPEN	-
5	RESERVE	-	-	-	-	OPEN	-
6	GND	-	-	-	-	-	-
7	GND	-	-	-	-	-	-
8	GND	-	-	-	-	-	-
9	GND	-	-	-	-	-	-
10	RF_IN	INPUT	-	-	-	OPEN	L1 & L5 band RF signal input pin
11	GND	-	-	-	-	-	-
12	NC	-	-	-	-	OPEN	-
13	NC	-	-	-	-	OPEN	-
14	VCC_ANT	Power Input	-	-	-	OPEN	Antenna Detector power supply / Antenna power supply input pin
15	GPIO2	OUTPUT [2)]	3.3V	-	Hi-Z	OPEN	Refer to Protocol Specifications
16	OCLK1	OUTPUT	3.3V		Hi-Z	OPEN	PPS/clock output pin
17	GND	-	-	-	-	-	-
18	NC	-	-	-	-	OPEN	Don't connect to GND.
19	GND	-	-	-	-	-	-
20	VBK	Power Input	-	-	-	OPEN	Backup power supply input pin
21	GND	-	-	-	-	-	-
22	GND	-	-	-	-	-	-
23	NC	-	-	-	-	OPEN	-
24	NC	-	-	-	-	OPEN	-
25	GND	-	-	-	-	-	-
26	GND	-	-	-	-	-	-
27	RESERVE	-	-	-	Hi-Z	OPEN	-
28	RESERVE	-	-	-	Hi-Z	OPEN	-
29	RX	INPUT	3.3V	PU	Hi-Z	OPEN or PU	UART reception input pin
30	TX	OUTPUT	3.3V	-	Hi-Z	OPEN	UART transmission output pin
31	GND	-	-	-	-	-	-
32	ICLK	INPUT	3.3V	PD	Hi-Z	GND or PD	PPS/clock input pin
33	OCLK2	OUTPUT	3.3V	-	Hi-Z	OPEN	PPS/clock output pin
34	GND	-	-	-	-	-	-
35	NC	-	-	-	-	OPEN	-
36	NC	-	-	-	-	OPEN	-
37	GND	-	-	-	-	-	-
38	OCLK0	OUTPUT	3.3V	-	Hi-Z	OPEN	PPS/clock output pin
39	GPIO0	OUTPUT [2)]	3.3V	-	Hi-Z	OPEN	Refer to Protocol Specifications
40	GPIO1	OUTPUT [2)]	3.3V	-	Hi-Z	OPEN	Refer to Protocol Specifications
41	RESERVE	-	-	-	-	OPEN	-
42	GND	-	-	-	-	-	-
43	VCC	Power Input	-	-	-	-	Main power supply input pin
44	Reset_X	INPUT	1.8V	PU	-	OPEN or PU	External reset signal input pin Logic L: Reset Logic H: Normal operation
45	GND	-	-	-	-	-	-
46	NC	-	-	-	-	OPEN	-
47	GND	-	-	-	-	-	-

Notes:
1) Pull-up and pull-down resistor values are shown in Table 5.3.
2) Hi-Z when command is not set.

5 Electrical Characteristics

5.1 Absolute Maximum Rating

The lists of absolute maximum ratings are specified over operating case temperature shown in Table 6.1. Stresses beyond those listed under those ranges may cause permanent damage to the module.

Table 5.1 Absolute Maximum Rating

Items	Symbol	Min.	Max.	Unit	Notes
Supply voltage to VCC	V_{CC_ABS}	-0.3	4.0	V	-
Supply voltage to VBK	V_{BK_ABS}	-0.3	2.5	V	-
Supply voltage to VCC_VANT	V_{ANT_ABS}	-	7.0	V	-
Digital input (DI) voltage	-	-0.3	3.7	V	-
Digital input (DI) voltage	-	-0.3	2.2	V	Apply to Reset_X pin.
RF_IN input power	$P_{\_RF\_ABS}$	-	0	dBm	-
Magnetic field strength	T_{MFS_ABS}	-	1000	mT	-

5.2 Power Supply

Table 5.2 Power Supply Characteristics

T_A=25°C, unless otherwise stated

Items	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply voltage to VCC	V_{CC0}	3.0	3.3	3.60	V	-
Supply voltage to VBK	V_{BK}	1.40	1.80	1.98	V	-
Supply voltage to VCC_VANT	V_{ANT}	3.0		5.0	V	-
VCC rising slew rate	V_{CC_RS}	0.2	-	20	ms	Figure 5.4.1
VCC current consumption	I_{CCAL}	-	55	200	mA	Full search @T_A=85°C
	I_{CCTL}	-	50	-	mA	Tracking satellite outdoor @T_A=85°C
VBK current consumption at back up	I_{BKN}	-	40	-	µA	V_{CC}=0V
		-	-	1.5	mA	V_{CC}=0V @T_A=85°C
VBK current consumption at normal operation)	I_{BKB}	-	-	0.1	µA	V_{CC}=3.3V

5.3 Digital Interface Signal

Table 5.3 Interface Signal

T_A=25°C, unless otherwise stated

Items	Symbol	Min.	Typ.	Max.	Unit	Notes
Logic L input voltage for 3.3V power domain Inputs	V_{IL}	0	-	0.3 x VCC	V	-
Logic H input voltage for 3.3V power domain Inputs	V_{IH}	0.7 x VCC	-	VCC	V	-
Logic L input voltage for 1.8V power domain Input (Reset_X)	V_{IL_RST}	0	-	0.5	V	Apply to Reset_X pin
Logic H input voltage for 1.8V power domain Input (Reset_X)	V_{IH_RST}	1.36	1.8	-	V	Apply to Reset_X pin
Logic L output voltage	V_{OL}	0	-	0.2 x VCC	V	@$\|I_{OL}\|$ = 2mA
Logic H output voltage	V_{OH}	0.8 x VCC	-	VCC	V	@$\|I_{OH}\|$ = 2mA
Pull-up resistor for 3.3V power domain I/O	R_{PU}	33	-	330	kΩ	-
Pull-up resistor for 1.8V power domain Input (Reset_X)	R_{PU_RST}	-	10	-	kΩ	Apply to Reset_X pin
Pull-down resistor	R_{PD}	33	-	330	kΩ	-

5.4 Operation Sequence

5.4.1 Rise Time for Power Supply

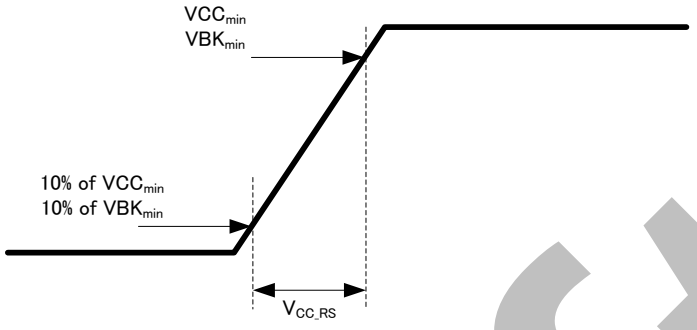


Figure 5.4.1 Rise Time for Power Supply Sequence

5.4.2 Power-up / Power-down timing of VBK and VCC

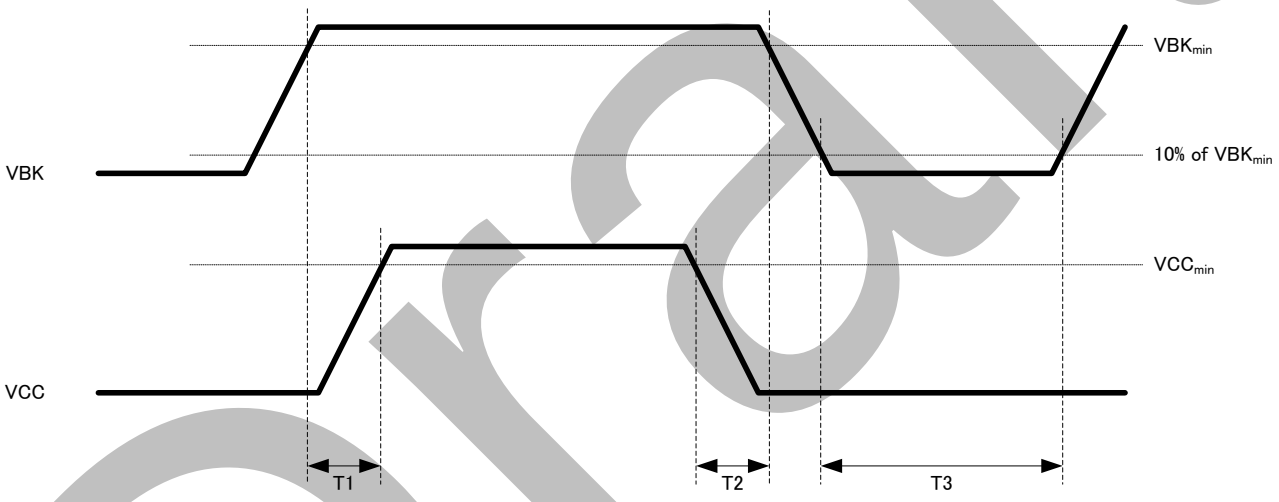


Figure 5.4.2 Power-up / Power-down timing of VBK and VCC Sequence

Table 5.4.2 Power-up / Power-down timing of VBK and VCC Sequence

Items	Symbol	Min.	Typ.	Max.	Unit	Notes
VBK rise to VCC rise time	T1	0	-	-	ms	The VBK should rise at earlier than or VCC rising.
VCC fall to VBK fall time	T2	0	-	-	ms	The VCC should fall earlier than or same timing as the VBK falling.
Minimum VBK inactive time	T3	500	-	-	ms	The VBK should be kept low more than 500ms.

5.5 Reset

5.5.1 External Reset

In most cases, it is not required to drive external reset input (Reset_X) pin. However, if it is needed to force the reset state externally for e.g. synchronizing the reset state with the application circuitry, Reset_X can be used for this purpose. The H voltage level of the Reset_X signal should be 1.8V. The Reset_X has an internal pull-up. (Pull-up resistor is 10kΩ.) An open-drain or open-collectors is recommended to prevent collisions with internal pull-up voltages.

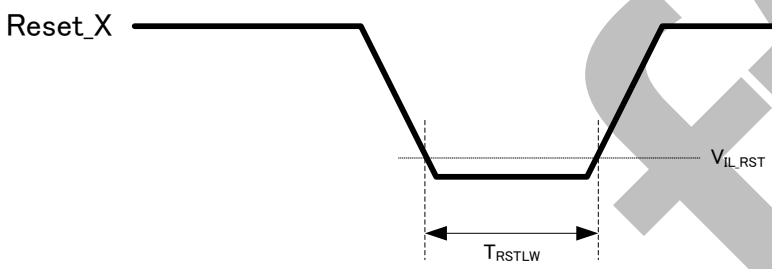


Figure 5.5.1 Reset Sequence

Table 5.5.1 Reset Sequence

Items	Symbol	Min.	Max.	Unit	Notes
Minimum reset activate time	T_{RSTLW}	500	-	ms	The Reset_X should be kept low more than 500ms.

5.5.2 UART Wake-up Timing after Reset

5.5.2.1 Without External Reset

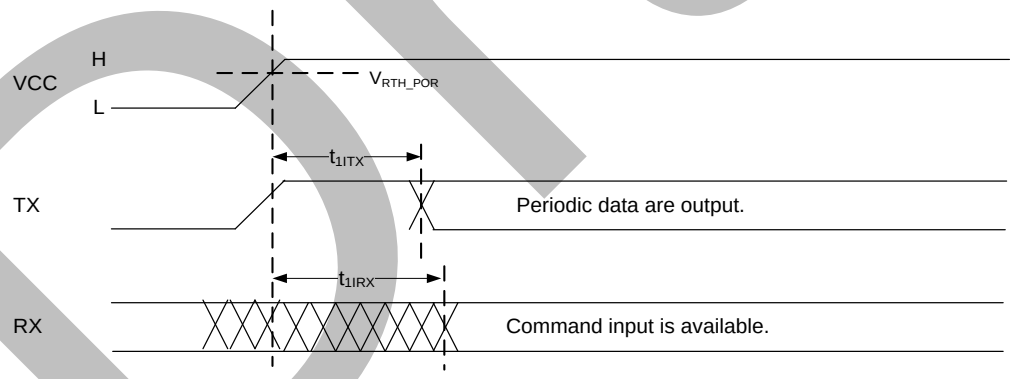


Figure 5.5.2.1 UART Wake-up Timing after V_{RTH_POR}

Table 5.4.2.1 UART Wake-up Timing after V_{RTH_POR}

Items	Symbol	Min.	Max.	Unit	Notes
Time delay from VCC reaches V_{RTH_POR} to TX valid	t_{1ITX}	-	6	s	
Time delay from VCC reaches V_{RTH_POR} to RX ready	t_{1IRX}	-	6	s	

5.5.2.2 With External Reset

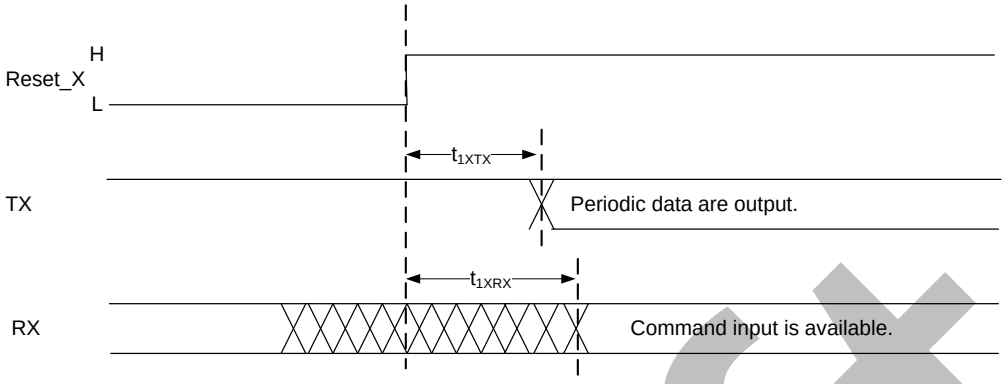


Figure 5.1.2.2 UART Wake-up Timing after Reset_X

Table 5.5.2.2 UART Wake-up Timing after Reset_X

Items	Symbol	Min.	Max.	Unit	Notes
Time delay from Reset_X set to H to TX valid	t_{1XTX}	-	6	s	
Time delay from Reset_X set to H to RX ready	t_{1XRX}	-	6	s	

5.6 Antenna

5.6.1 Recommended Antenna

Table 5.6.1 Recommended Active Antenna

Item	Min.	Typ.	Max.	Unit	Remarks
L1 Bandwidth	1559	-	1606	MHz	
L5 Bandwidth	1166	-	1187	MHz	
Antenna element gain	0	-	-	dBi	
Amplifier gain	15	-	50	dB	Including cable loss. 15 dB to 25 dB is recommended for noise robustness
Amplifier NF	-	-	3	dB	Including cable loss
Impedance	-	50	-	Ω	

5.6.2 Antenna Amplifier Power

Power for antenna pre-amplifier input on pin #14 (VCC_ANT) is superimposed (biased) on pin #10 (RF_IN).

GT-100 have the function of supplying voltage to the active antenna and diagnosing the connection state (open, short) of the antenna. The diagnostic results are output by the proprietary NMEA message. In addition, it also has a protection function (OFF Mode) when the antenna is shorted. To return from OFF mode to the Normal Mode, please turn off the power supply voltage to VCC_ANT and remove what is causing the Antenna short state. Once the Off Mode condition is recovered, the mode will be change to Normal Mode when VCC_ANT is resupplied.

Table 5.6.2 Recommended Antenna Power

T_A=25°C, VCC_ANT=5V unless otherwise stated

Items	Symbol	Min	Typ	Max	Unit	Notes
Output voltage	V_{APO}	V_{ANT}-0.5	-	-	V	@ I_{APO}=50mA
Output current	I_{APO}	-	-	55	mA	-
Open Detect Threshold Current	I_{AOD}	-	1.3	2.5	mA	-
Short Detect Threshold Current	I_{ASD}	60	82	-	mA	-
Short Protection	I_{ASP}	68	-	130	mA	-
Load Capacity	C_{ALC}	-	-	50	μF	

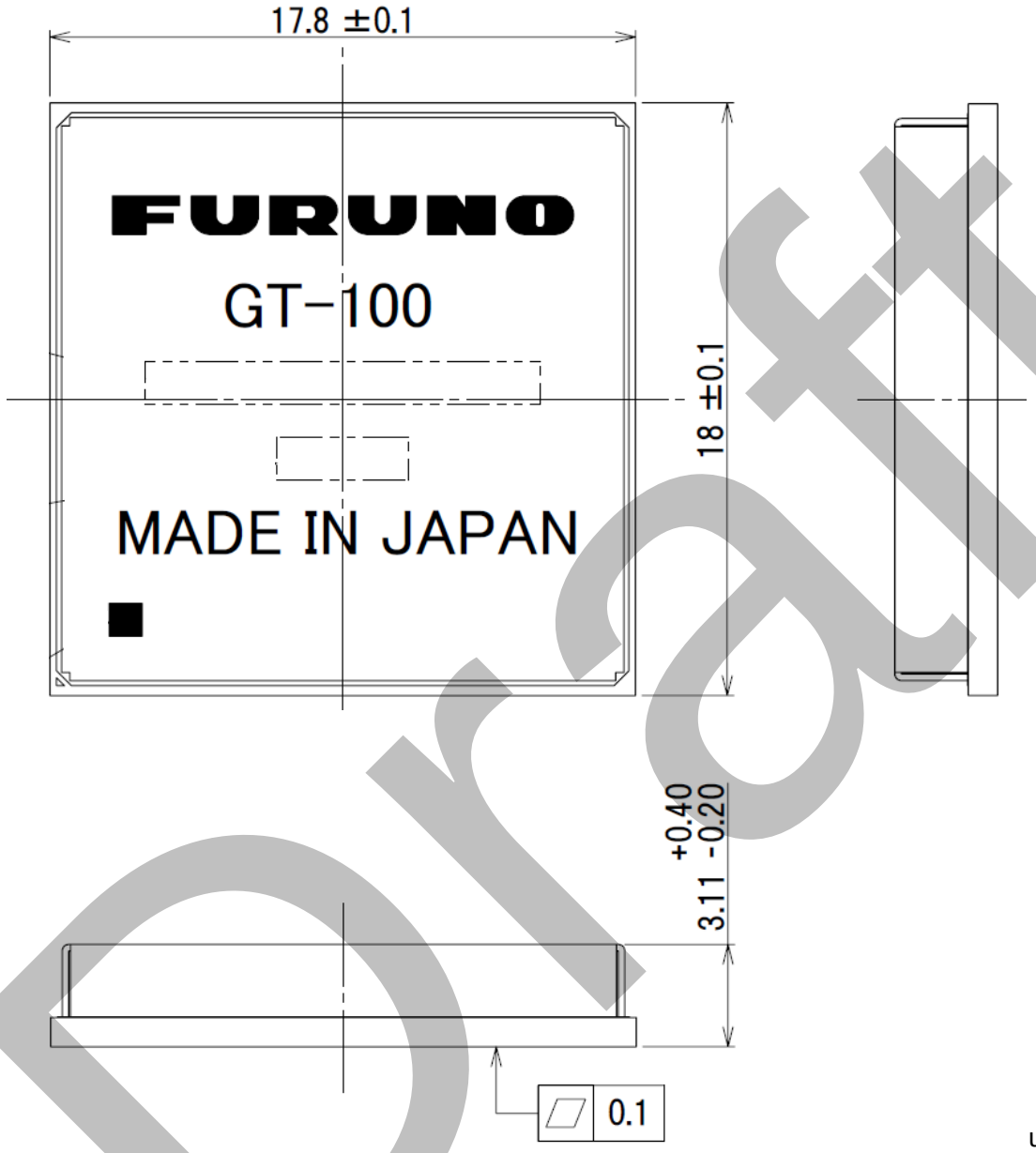
6 Environmental Specifications

Table 6.1 Environmental Specifications

Items		Specification	Unit	Notes
Operating temperature		-40 to +85	°C	-
Storage temperature		-40 to +105	°C	-
Magnetic field immunity	10-year data retention	Max 100	mT	@25°C
		Max 90	mT	@55°C
		Max 55	mT	@85°C
	Active Read / Write	Max 25	mT	-

7 Mechanical Specifications

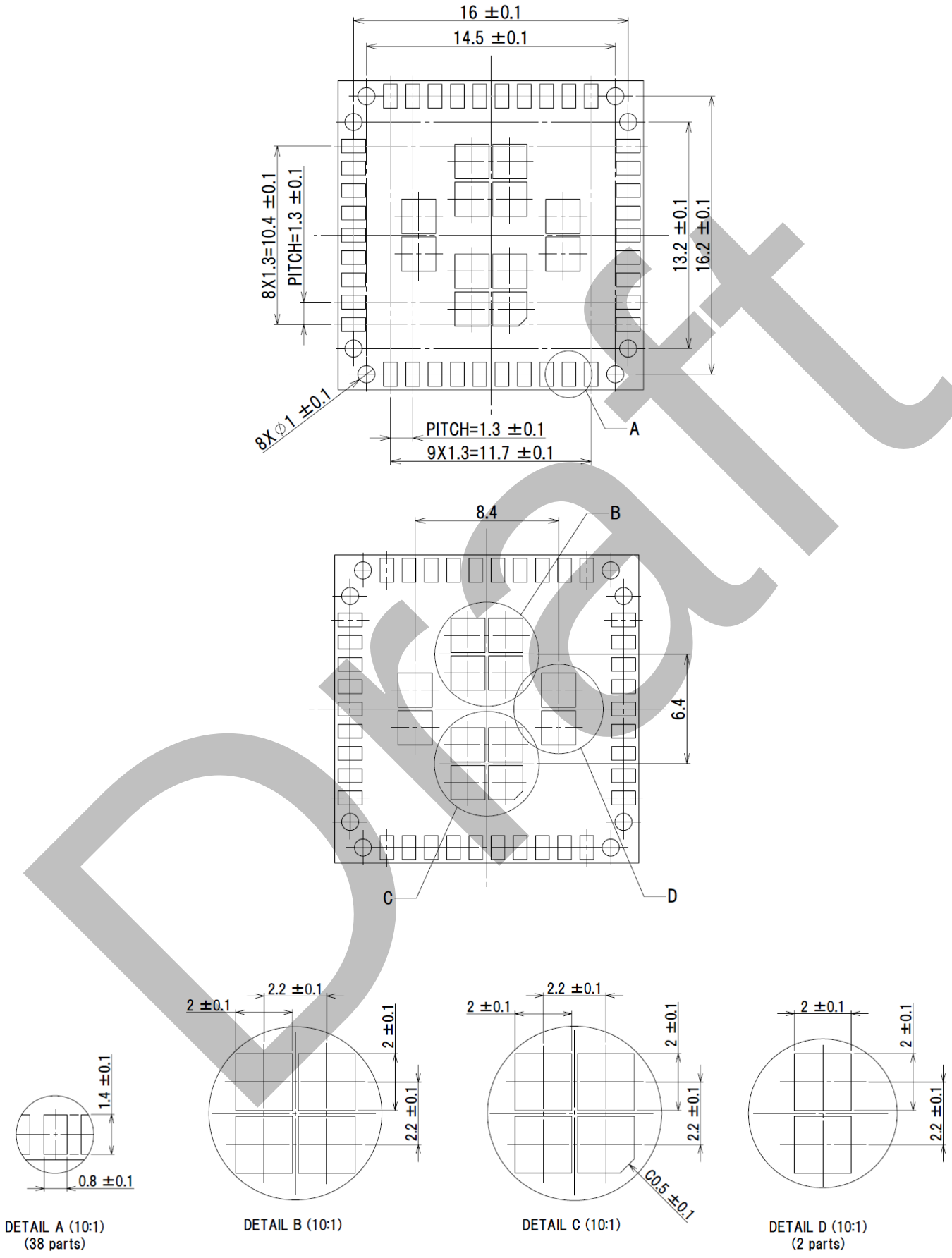
7.1 Mechanical Description



units: [mm]

Note: Tolerances are ±0.3mm, unless otherwise specified.
Dimensions in ( ): It is reference dimension.
The terminal coplanarity of product assumes the state of room temperature.

units: [mm]


16 ±0.1
14.5 ±0.1
8X1.3=10.4 ±0.1
PITCH=1.3 ±0.1
13.2 ±0.1
16.2 ±0.1
8X φ1 ±0.1
PITCH=1.3 ±0.1
9X1.3=11.7 ±0.1
A
8.4
B
6.4
C
D
1.4 ±0.1
0.8 ±0.1
DETAIL A (10:1)
(38 parts)
2.2 ±0.1
2 ±0.1
2 ±0.1
2.2 ±0.1
DETAIL B (10:1)
2.2 ±0.1
2 ±0.1
2 ±0.1
2.2 ±0.1
C0.5 ±0.1
DETAIL C (10:1)
2 ±0.1
2 ±0.1
2.2 ±0.1
DETAIL D (10:1)
(2 parts)

Note: Tolerances are ±0.3mm, unless otherwise specified.
Dimensions in ( ): It is reference dimension.
The terminal coplanarity of product assumes the state of room temperature.
Alps Alpine Lot Number shall be conformed to Alps Alpine numbering rules.
Surface treatment specifications for module bottom terminal.
Material : Cu
Surface finish : Ni-Au
Ni 3µm - 8µm
Au 0.05µm – 0.15µm

7.2 Weight

1.7g (TYP)

8 MECHANICAL DESIGN INFORMATION

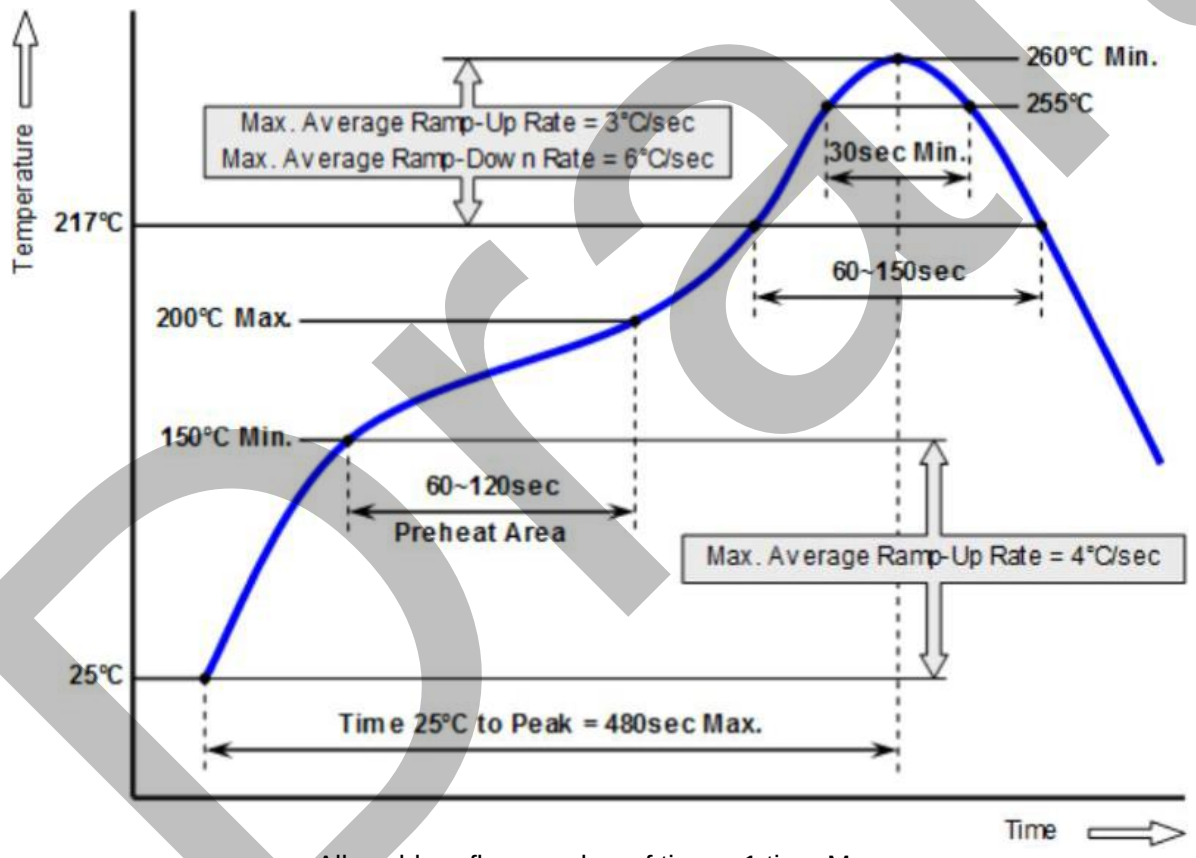
Recommended Copper Land and Solder Stop Mask (Resist) on Customer's Mother Board and Solder Print Mask (Metal Mask) Dimensions for better soldering with GT-100. The following drawings have been verified based on FURUNO recommended reflow soldering conditions and reference PCB. The reflow solderability should vary in accordance to the thickness of the PCB, reflow condition and pattern layout etc. If the customer will apply these conditions (Cupper Land, Solder Stop Mask, Solder Print Mask, etc.), further verification or modification of these parameters may be necessary. Please solder the NC pins to NC footprint patterns of the Main Board.

8.1 Refollow times

1 time

Note: This Module is exclusive use of reflow

8.2 Reflow Heat Resistance



Allowable reflow number of times: 1 time Max.

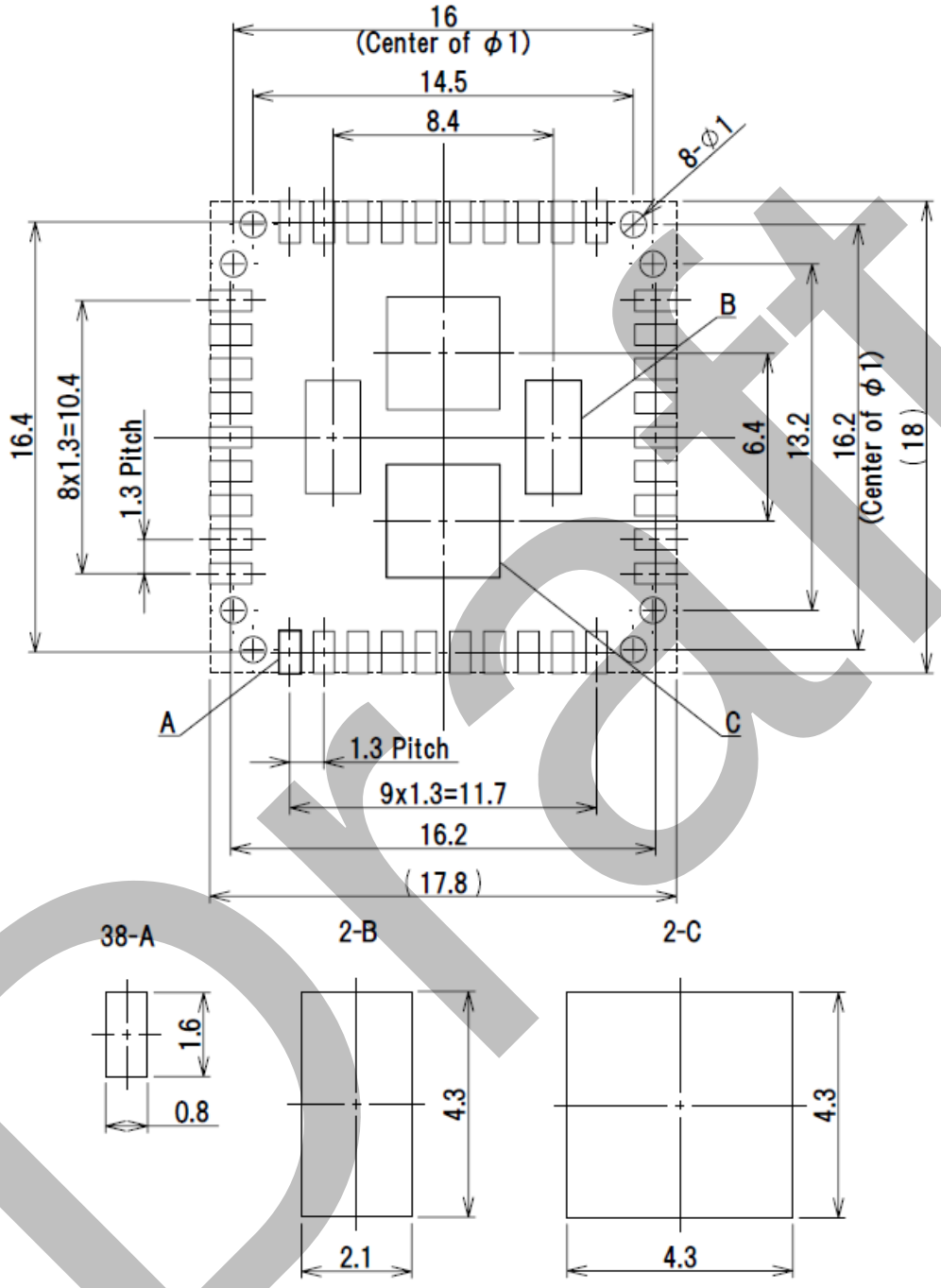
Note:
1. The measurement point is at the center of the upper surface of the module.
2. Please execute the reflow soldering on the following conditions according to JEDEC J-STD-020D.
Peak Temperature: Max. 260[°C]
Peak Time (≥ 255[°C]): Max. 30[s]

8.3 Storage Conditions

The following conditions shall be kept for soldering and keeping in storage this product.

1. Shelf life in dry bag: 12 months at 5 ~ 40 °C and < 85 % RH.
2. After dry bag is opened, module that will be subjected to soldering reflow or equivalent processing must be:
   a) Mounted within 168 hours at factory condition of < 30 °C / 60 % RH, or
   b) Stored at < 30 °C / 10 % RH.
3. Modules require baking, before mounting, if:
   a) Humidity Indicator Card is >10 % when read at 23 °C ± 5 °C, or
   b) Item 2.a) or 2.b) are not met.
4. If baking is required, device may be baked for 216 hours at 40 ~ 45 °C and < 5 % RH for low-temperature device containers.
   a) Allowable baking number of times: 1time.

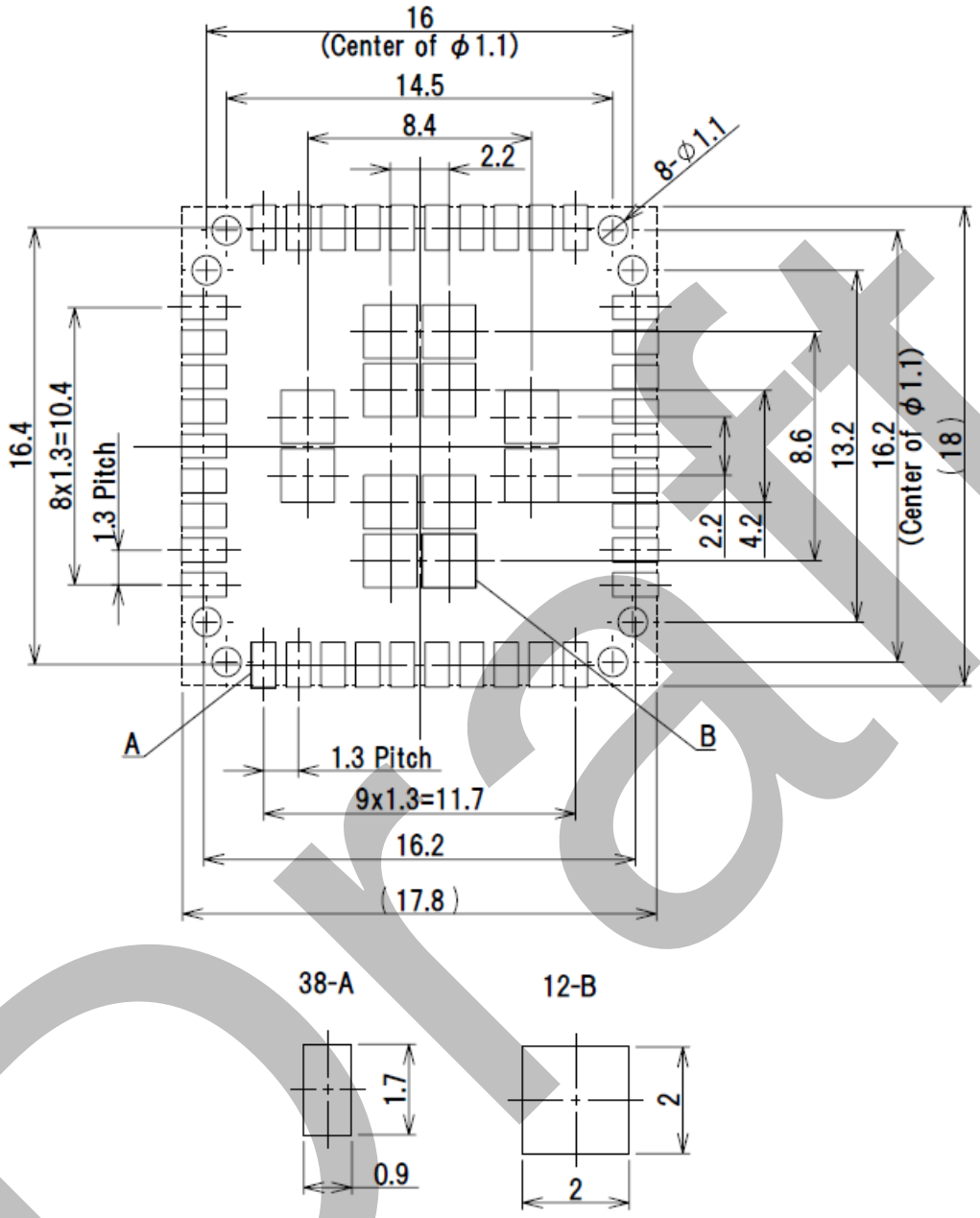
8.4 Copper Land Design



units: [mm]

Note
1. All are Top View.
2. Recommended Pattern and Solder stop mask on Customer's board and Metal mask dimensions for better soldering with GT-100.
3. Tolerances are ±0.1mm, unless otherwise specified.

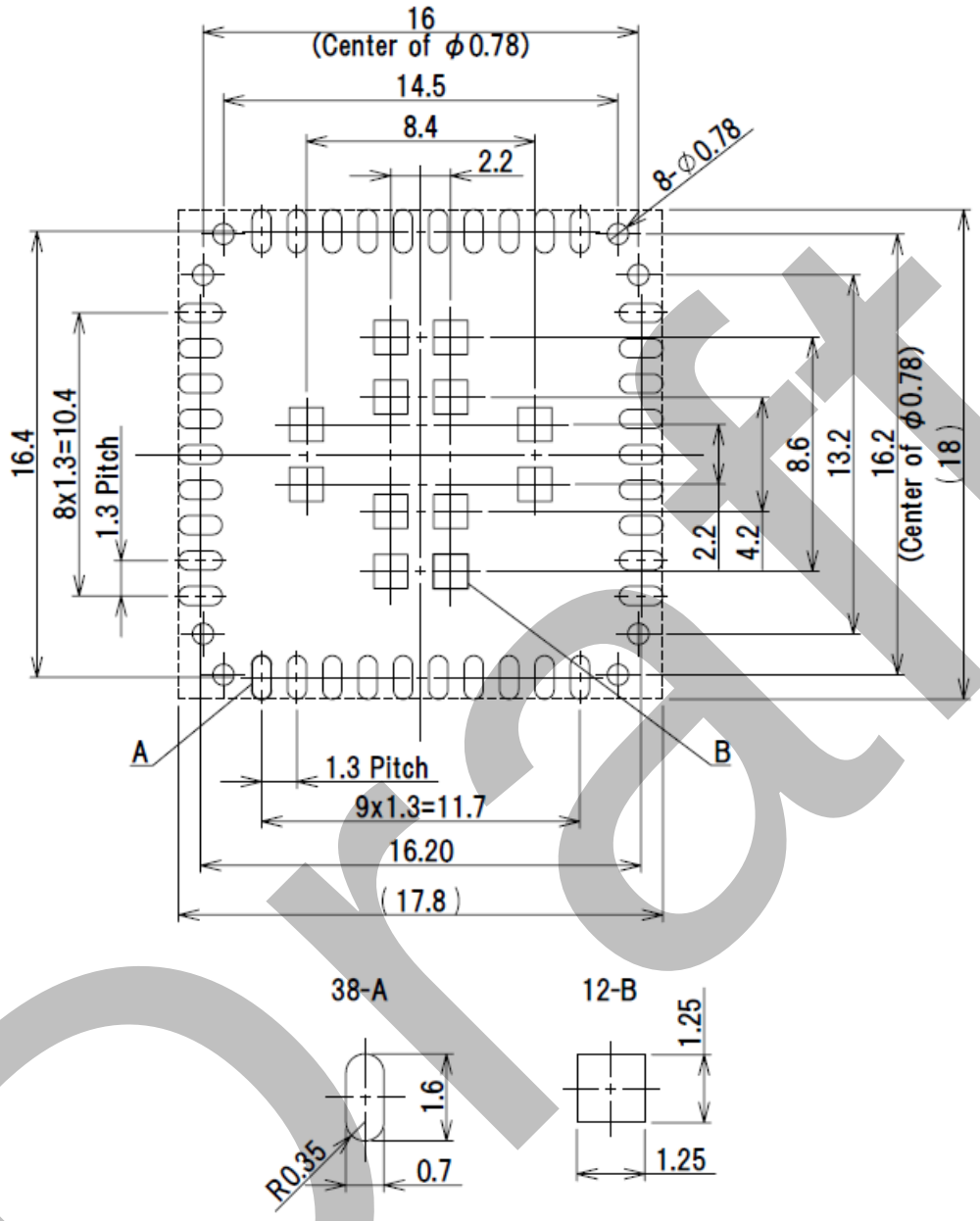
8.5 Solder Stop Mask Design



units: [mm]

Note
1. All are Top View.
2. Recommended Pattern and Solder stop mask on Customer's board and Metal mask dimensions for better soldering with GT-100.
3. Tolerances are ±0.1mm, unless otherwise specified.

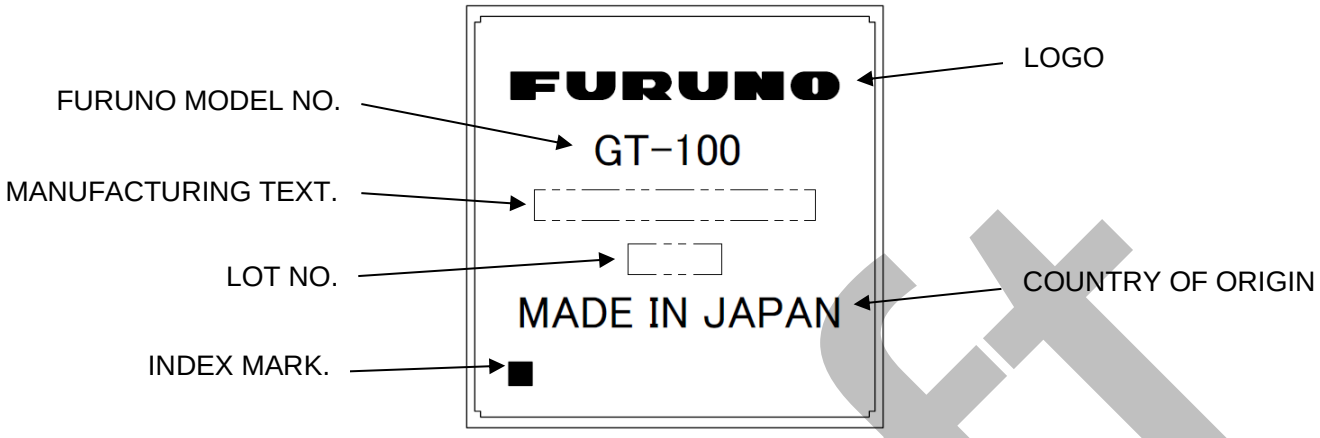
8.6 Solder Print Mask Design



units: [mm]

Note
1. All are Top View.
2. Recommended Pattern and Solder stop mask on Customer's board and Metal mask dimensions for better soldering with GT-100.
3. Tolerances are ±0.1mm, unless otherwise specified.

9 Marking



Items	Description
LOGO	FURUNO
FURUNO MODEL NO	GT-100
MANUFACTURING TEXT	The twelve digits max "UMSZ6□□□□□□"
LOT NO	The three digits "□□□" Time Bucket(A~E) Month Code Jan 1, Feb 2, Mar 3, Apr 4, May 5, Jun 6 Jul 7, Aug 8, Sep 9, Oct 10, Nov 11, Dec 12 Year Code CY2022 2, CY2023 3, CY2024 4 Note: Last number of Christian years.
COUNTRY OF ORIGIN	MADE IN JAPAN

10 Special Instruction

10.1 Electronic Component

Components in GT-100 module such as chip resistors, capacitors and TCXO's are planned to be purchased from multiple manufacturers/vendors according to FURUNO's procurement policy. So it is possible that multiple components from multiple manufacturers/vendors could be used even in the same production lot.

10.2 RoHS

GT-100 comply with RoHS directives.

11 Reference Documents

- FURUNO SE22-600-013 GT-100 Function Specifications
- FURUNO SE22-600-007 GT-100 PFEC Protocol Specifications