FURUNO

FURUNO Multi-GNSS Disciplined Oscillator

GF-8701,GF-8702,GF-8703

Hardware Specifications

(Document No.G14-000-10-029-1)

Preliminary

FURUNO ELECTRIC CO., LTD.

www.furuno.co.jp

FURUNO ELECTRIC CO., LTD. reserves the right to make changes to its products and specifications without notice.

All brand and product names are registered trademarks, trademarks or service marks of their respective holders.

The following satellite systems are operated and controlled by the authorities of each government.
- GPS(USA)
- GLONASS(Russia)
- Galileo(Europe)
- QZSS(Japan)
- SBAS(USA: WASS, Europe: EGNOS, Japan: MSAS)

Thus FURUNO is not liable for the degradation of the above systems so therefore FURUNO cannot guarantee specification based on their conditions. User is expected to be familiar with the system and make full use of it with their own responsibility.

Note!

These products are currently under development. The contents described this document may change because we are improving the performance and correcting it without announcements.

Revision History

Revision#	Revised description	Date
0	Preliminary & Confidential Release	2015.01.05
1	Removed the watermark “Preliminary & Confidential” which was printed e very page. Corrected some typos.	2015.02.09

Table of Contents

1 Outline

GF-8701, GF-8702 and GF-8703 are FURUNO Multi-GNSS disciplined oscillators (*1). Main features are as follows.

- Supports GPS, SBAS, GLONASS and QZSS (*2)
- Provides high accuracy PPS signal synchronized with UTC
- Provides the clock (10 MHz) synchronized with PPS
- Software upgrade capability by Flash ROM
- Active Anti-jamming capability to suppress effects of CW jammers
- Multi path mitigation effects
- GPS high sensitivity (-161 dBm (Hot acquisition))
- These Multi-GNSS disciplined oscillators are pin compatible. (*3)

Notes:
(*1) This document abbreviates Multi-GNSS Disciplined Oscillator to GNSSDO.
(*2) These satellite system is called as GNSS collectively.
(*3) The specifications of the power consumption, PPS and 10 MHz are different.

2 Block Diagram

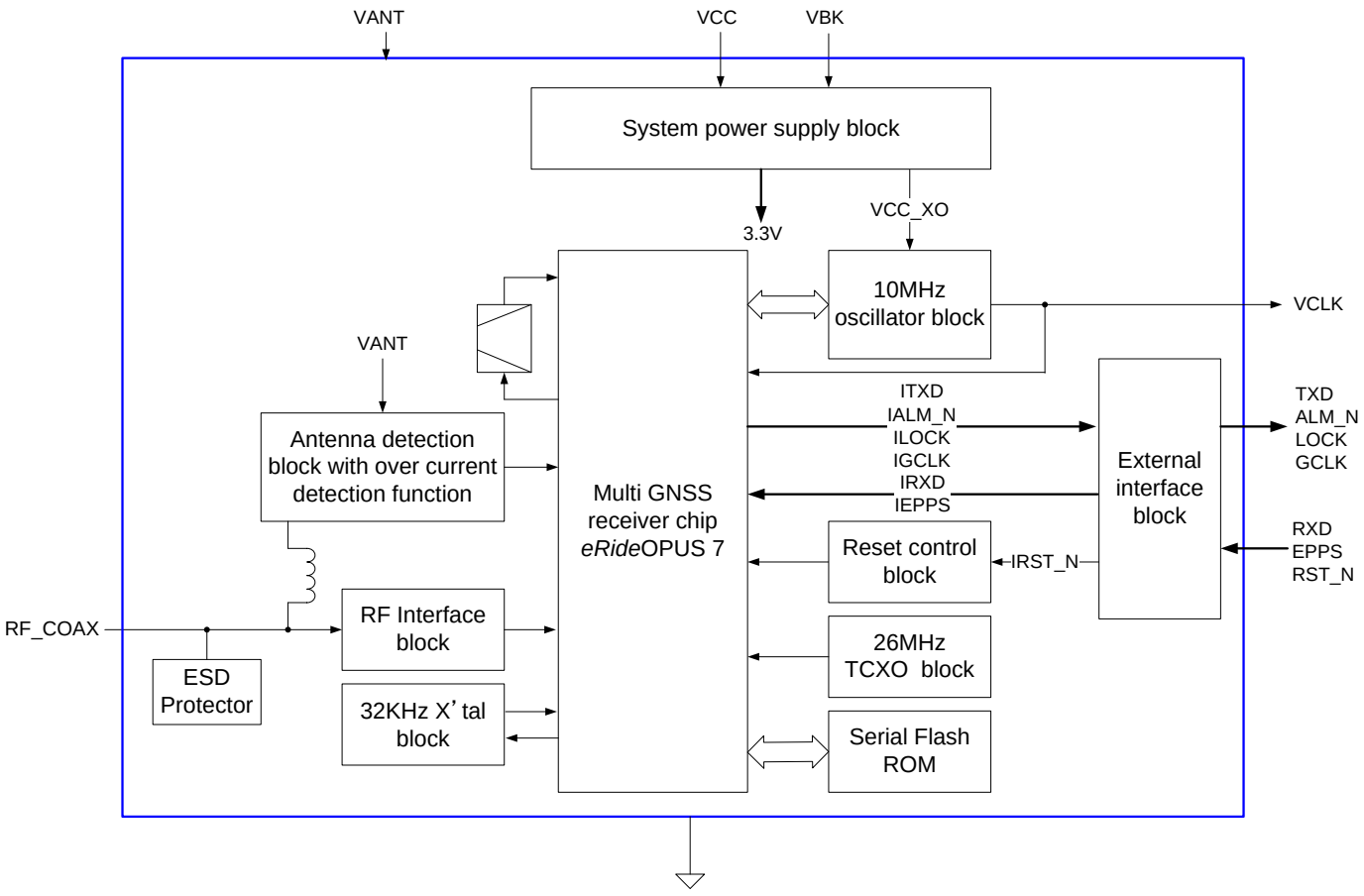


Figure 3.1 GF-8701/GF-8702/GF-8703 Block Level Diagram

3 GNSS General Specification

Table 3.1 GNSS General Specifications

Items	Description		Notes
GNSS reception capability	GPS L1C/A	12	
	SBAS L1C/A	2	WAAS, MSAS, EGNOS, GAGAN
	GLONASS L1OF	10	
	QZSS L1C/A	2	
GNSS concurrent reception	GPS, SBAS, GLONASS and QZSS	26	
Environment robustness performance	Active Anti-jamming	8CW	
	Multipath Mitigation	●	
Serial data format	NMEA	●	Ver. 4.10, Default 38400 bps (*1)
Antenna	Active Antenna	●	
Operation limit	Altitude	18,000m	Compliant with the Wassenaar Arrangement Specifications
	Velocity	515 m/s	

Notes:
(*1): See the protocol specifications for details.

4 GNSS General Performance

Table 4.1 General Performance

T_A=25°C

Items	Description		Notes
TTFF	Hot Outdoor	<5 sec	These are specified with the measurement platform shown in Figure 4.1. Simulator output level is set to -130 dBm.
	Warm Outdoor	35 sec	
	Cold Outdoor	35 sec	
GPS sensitivity	Tracking	-161 dBm	These are specified with the measurement platform shown in Figure 4.1.
	Hot Acquisition	-161 dBm	
	Cold Acquisition	-147 dBm	
	Reacquisition	-161 dBm	
GLONASS sensitivity	Tracking	-157 dBm	
	Hot Acquisition	-157 dBm	
	Cold Acquisition	-143 dBm	
	Reacquisition	-157 dBm	
Position Accuracy	Horizontal Outdoor	2.5m CEP	GPS only Open sky 24 hours with recommended antenna
		2.0m CEP	GPS, GLONASS and SBAS Open sky 24 hours with recommended antenna

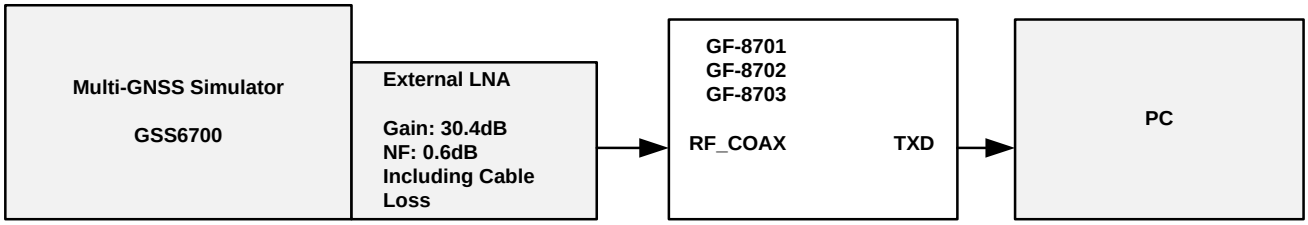


Figure 4.1 Measurement Platform

5 I/O Signal Description

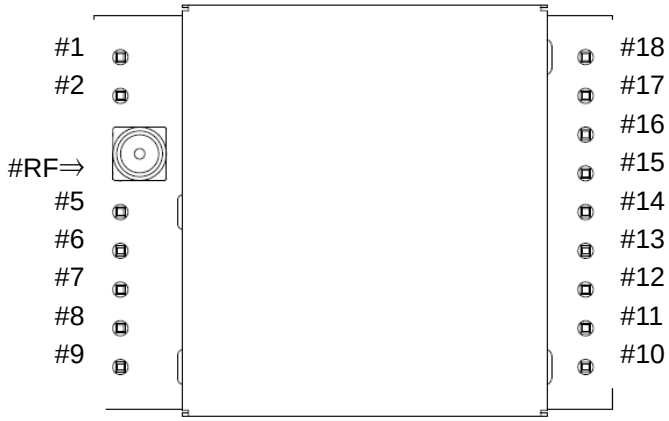


Figure 5.1 Top of view

Table 5.1 I/O Signal Description

#	Pin Name	Type	PU/PD(*1)	Description
1	RST_N	Digital input	Pull-up	External reset signal input pin Logic L : Reset Logic H or Open : Normal Operation
2	VANT	Power Input	-	Power supply output pin for active antenna
5	GND	-	-	Ground
6	RESERVE	-	-	Open this pin
7	GND	-	-	Ground
8	VBK	Power Input	-	Backup power supply input pin (*2) Do not connect or connect to GND or VCC if battery backup function is not used
9	VCC	Power Input	-	Main power supply input pin
10	GND	-	-	Ground
11	VCLK	Digital output	-	VCO clock output pin (10MHz)
12	RXD	Digital input	Pull-up	Serial communication input pin
13	TXD	Digital output	-	Serial communication output pin
14	ALM_N	Digital output	-	Alarm signal output pin (*3) Logic L : Abnormal Logic H : Normal
15	LOCK	Digital output	-	Lock signal output pin (*4) Logic L :Unlock Logic H :Lock
16	GCLK	Digital output	-	Clock output pin (from 4kHz to 40MHz)
17	PPS	Digital output	-	Pulse per second output pin
18	EPPS	Digital input	Pull-down	External synchronized PPS input pin
RF	RF_COAX	Analog input	-	RF signal input connector Power for antenna pre-amplifier is super-imposed (biased) from this connector (default). MMCX connector receptacle /50Ω

Notes:
(*1) Pull-up and pull-down register values are shown in Table 6.3.

(*2) The backup power is shown in section 8.4.
(*3) The alarm output conditions are shown in section 8.1.
(*4) The lock output conditions are shown in section 8.2.

6 Electrical Specifications

6.1 Absolute Maximum Rating

The lists of absolute maximum ratings are specified over Operating Temperature shown in Table 10.1. Stresses beyond those listed under those range may cause permanent damage to module.

Table 6.1 Absolute Maximum Rating

Items	Symbol	Min	Max	Unit	Notes
VCC supply voltage	V_{CC}	-0.3	6.0	V	
VANT supply voltage	V_{ANT}	-0.3	6.0	V	
Backup voltage	V_{BK}	-0.3	4.0	V	
Other pins DC voltage	V_{IN}	-0.5	7.0	V	Input voltage
	$V_{I/O}$	-0.5	7.0	V	at power down
		-0.5	3.8	V	Output high level or low level
Other pins DC current	-	-	±50	mA	

6.2 Power Supply

Table 6.2 Power Supply Characteristics

T_A=25°C unless otherwise stated

Items		Symbol	Min.	Typ	Max	Unit	Notes
Supply voltage to pin VCC		V_{CC}	3.5	3.7	3.9	V	
Supply voltage to pin VANT		V_{ANT}	-	-	5.5	V	
Backup supply to pin VBK		V_{BK}	1.4	-	3.6	V	at using VBK
Rising slew rate of VCC		V_{CC_SR}	-	-	$3.9x10^4$	V/s	See Figure 6.2
Rising slew rate of VBK		V_{BK_SR}	3.6	-	$3.6x10^4$	V/s	See Figure 6.2
VCC current consumption (at start up)	GF-8701	I_{CC_WU01}	-	-	150	mA	
	GF-8702	I_{CC_WU02}	-	-	800	mA	
	GF-8703	I_{CC_WU03}	-	-	1400	mA	
VCC current consumption (at stable state)	GF-8701	I_{CC_ST01}	-	-	150	mA	
	GF-8702	I_{CC_ST02}	-	450	-	mA	
	GF-8703	I_{CC_ST03}	-	600	-	mA	
VBK current consumption at back up		I_{BKN}	-	9	TBD	µA	V_{CC}=0V
VBK current consumption at normal operation		I_{BKB}	-	0.4	2	µA	V_{CC}=5.5V

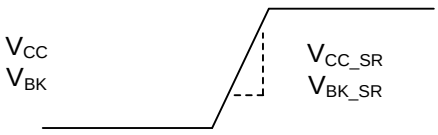


Figure 6.2 VCC/ VBK rising slew rate

6.3 Interface Signal

Table 6.3 Interface Signal

T_A=25°C, unless otherwise stated

Items	Symbol	Min	Typ	Max	Unit	Notes
Low-Level input voltage	V_{IL}	-	-	0.8	V	
High-Level input voltage	V_{IH}	2.0	-	5.5	V	
Low-Level output voltage	V_{OL}	-	-	0.4	V	I_{OL} = 16mA
High-Level output voltage	V_{OH}	2.4	-	3.6	V	I_{OH} = -18mA
Digital input pull-up resistor	R_{PU}	-	10	-	kΩ	
Digital input pull-down resistor	R_{PD}	-	10	-	kΩ	
Digital input pull-up voltage	V_{PU}	-	3.3	-	V	

6.4 Reset

6.4.1 Internal Power-on Reset

eRideOPUS 7 contains internal power-on reset circuit which detects VCC voltage and creates POR_N (power-on reset) signal for initializing module. Table 6.4.1 shows the threshold voltages to detect and create POR_N signal.

Table 6.4.1 Interface Signal

T_A=25°C, unless otherwise stated

Items	Symbol	Min	Typ	Max	Unit	Notes
Power On reset threshold voltage (rising)	V_{RTH_POR}	-	-	3.3	V	
Power On reset threshold voltage (falling)	V_{FTH_POR}	2.7	-	-	V	

6.4.2 External Reset

eRideOPUS7 is controlled by external reset signal (RST_N) with the following sequence.

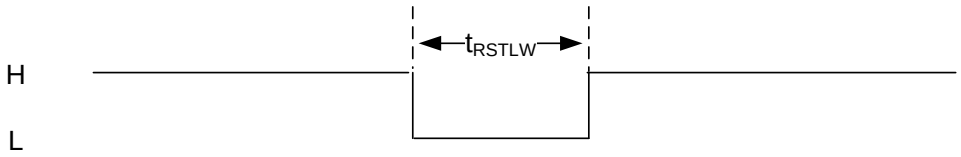


Figure 6.4.2. Reset Sequence

Table 6.4.2. Reset Sequence

Items	Symbol	Min	Max	Unit	Notes
RST_N pulse width	t_{RSTLW}	300	-	ms	

6.5 UART Wake-up Timing after Reset

6.5.1 Internal Reset Control

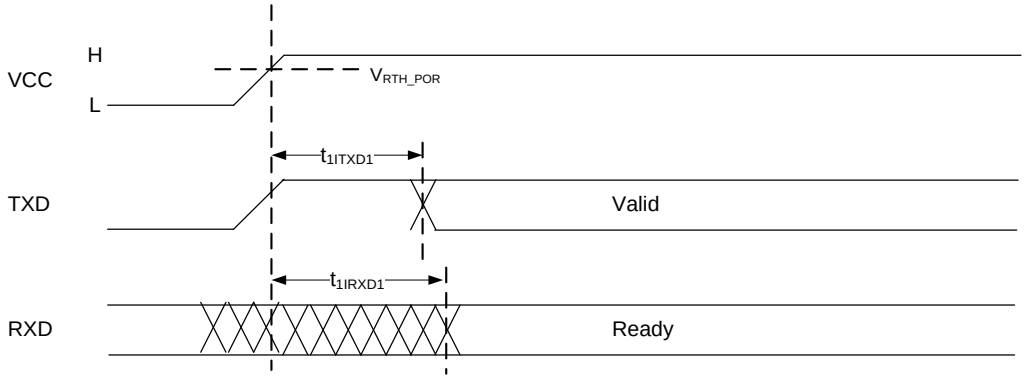


Figure 6.5.1 UART Wake-up Timing after VRTH_POR

Table 6.4.1 UART Wake-up Timing after VRTH_POR

Items	Symbol	Min	Max	Unit	Notes
Time delay from VCC reaches VRTH_POR to TxD1 valid.	t_{1ITXD1}	-	6	s	
Time delay from VCC reaches VRTH_POR to RxD1 ready.	t_{1IRXD1}	-	6	s	

6.5.2 External Reset Control

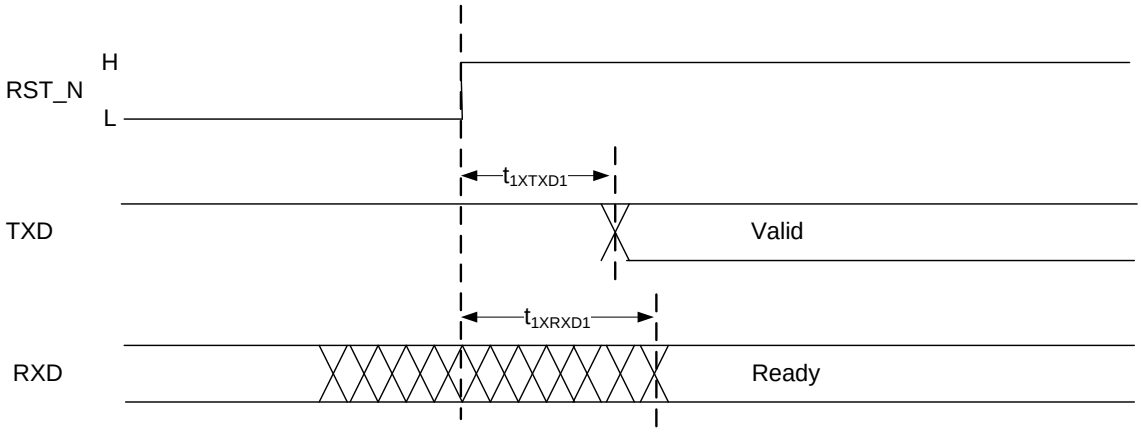


Figure 6.5.2 UART Wake-up Timing after RST_N

Table 6.5.2 UART Wake-up Timing after RST_N

Items	Symbol	Min	Max	Unit	Notes
Time delay from RST_N set to H to TXD valid.	t_{1XTXD1}	-	6	s	
Time delay from RST_N set to H to RXD ready.	t_{1XRXD1}	-	6	s	

6.5.3 Baud Rate Setting

The baud rate clock is created from 71.5 MHz system clock, hence it has some deviation errors against ideal baud rate clock as shown in Table 6.5.3.

Table 6.5.3 Baud Rate vs Deviation Error

Baud rate [bps]	Deviation error [%]
4800	0.00
9600	0.11
19200	-0.11
38400	0.32
57600	-0.54
115200	-0.54
230400	2.08
460800	-3.02

6.6 Antenna

6.6.1 Recommended Antenna

Table 6.5.1Recommended Antenna

Items	Min	Typ	Max	Unit	Notes
GPS center frequency	-	1575.42	-	MHz	2.046 MHz bandwidth
GLONASS center frequency	-	1602	-	MHz	9 MHz bandwidth
Antenna element gain	0	-	-	dBi	
Pre-amplifier gain	10	-	35	dB	Including cable loss
Pre-amplifier NF	-	-	3.5	dB	
Impedance	-	50	-	Ω	
VSWR	-	-	2	-	

6.6.2 Antenna Amplifier Power

Power for antenna pre-amplifier input from I/F pin #2 (VANT) is superimposed (biased) from the RF connector . The power supply is ON by default and it is able to be stopped the power supply with the command.

GF-8701/8702/8703 incorporates an antenna current error sensing function. In case of detecting an antenna current error, the alarm (ALM_N) is output. If the error is an antenna short (an over current), the antenna pre-amplifier power supply is stopped.

Table 6.6.2Recommended Antenna Power

Items	Symbol	Min	Typ	Max	Unit	Notes
Antenna pre-amplifier output voltage	V_{APO}	V_{ANT}-0.5	-	-	V	@ I_{APO}=75mA
Antenna pre-amplifier output current	I_{APO}	-	-	75	mA	
Threshold current of antenna open	I_{AOD}	-	5	10	mA	
Threshold current of antenna short	I_{ASD}	80	85	-	mA	

7 VCLK・GCLK・PPS Signal Specification

7.1 GNSS Locked State

Table 7.1 shows the specifications of GNSS locked state.

Table 7.1 GNSS Locked State Specifications

VCC=3.7V

Symbol	Items		Specification	Unit	Notes
VCLK	Frequency		10	MHz	Temperature gradient: ±20°C/h
	Frequency accuracy (24 hour average)	GF-8701	<±1E-11	-	
		GF-8702	<±1E-12		
		GF-8703	<±1E-12		
	Short term stability (Root Allan variance (τ =1s))	GF-8701	<1E-9	-	
		GF-8702	<2E-10	-	
		GF-8703	<2E-10	-	
GCLK	Frequency variable range		0.004 to 40	MHz	Open Sky
	Frequency accuracy		TBD		
	Total jitter		<8	ns	
PPS	Frequency		1	Hz	
	Duty ratio		50	%	
	PPS accuracy		<±100	ns	
	PPS stability (1 sigma)		<15	ns	

7.2 Holdover

Table 7.2 shows the specification of holdover when GF-8701/GF-8702/GF-8703 is not able to get the GNSS time data.

Table 7.2 Holdover Specifications

VCC=3.7V

Symbol	Items		Specification	Unit	Notes
VCLK	Frequency		10	MHz	Ambient temperature change: 20 °C Temperature gradient: +/- 5 °C/h Integrated value of temperature variation(*1) : 240 H * °C Before moving to Holdover mode, time to “Fine Lock” should be more than 72 hours and the time of power on should be more than 7 days.
	Frequency accuracy	GF-8701	TBD	-	
		GF-8702	<±3E-9	-	
		GF-8703	<±1E-9	-	
	Short term stability (Root Allan variance (τ =1s))	GF-8701	<1E-9	-	
		GF-8702	<2E-10	-	
		GF-8703	<2E-10	-	
GCLK	Frequency variable range		0.004～40	MHz	
	Frequency accuracy		TBD		
	Total jitter		<8	ns	
PPS	Frequency		1	Hz	
	Duty ratio		50	%	
	Timing accuracy (after 24 hour)	GF-8701	-	-	
		GF-8702	<±50	us	
		GF-8703	<±10	us	

Notes:
(*1)Integrated value of temperature variation from beginning of Holdover.

7.3 Time to “Fine Lock”

Table 7.3 shows the time to “Fine Lock” from power-on to GNNS lock.

Table 7.3 Fine Lock Specifications

T_A=25°C, unless otherwise stated

VCC OFF time	VBK state	State before VCC OFF	Adjusting time
5 s and more	-	-	・vs GPS: < 5 min ・vs UTC: < 15 min
less than 5 s	N/A		
	Available	Other than the below state	
		Power on time is more than 24 hour at GNSS lock state	・vs GPS: < 5 min ・vs UTC: < 5 min

7.4 PPS, VCLK, UART Output Phase

Figure 7.4 shows Output phase relation among PPS, VCLK and TXD. See the protocol specifications about the serial data output.

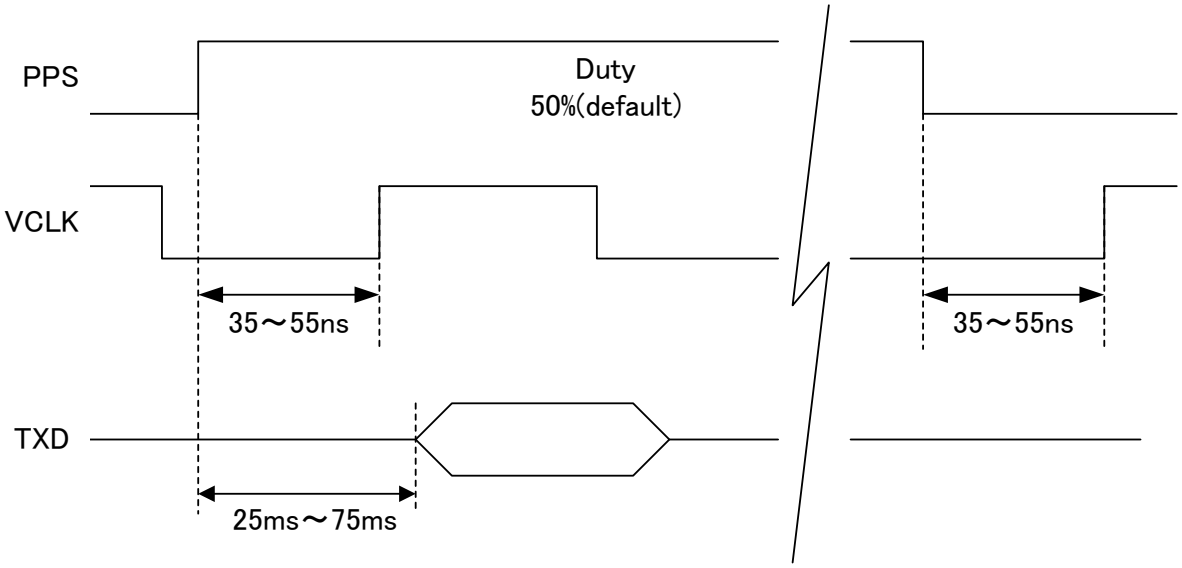


Figure 7.4 PPS, VCLK, UART Output Phase Relation

Notes:
The above figure shows a output phase relation between PPS and TXD after the frequency mode has become Pull-in. It does not show a phase relation during warm up.

8 Interface Signal Specification

8.1 Alarm Signal (ALM_N)

It is able to confirm the alarm signal (ALM_N) status by "alarm" field in CRZ (TP4) sentence. Table 8.1 shows the protocol specifications of alarm signal

Table 8.1 Alarm Signal Specifications

CRZ(TPS4) “alarm field”	ALM_N pin	Description
00	Logic H	Normal
Other than 00	Logic L	Abnormal

8.2 Lock Signal (LOCK)

It is able to confirm the lock signal (Lock) status by "frequency mode" field in CRZ (TP4) sentence and to set the lock pin output condition by "Lock post set" field in MODESET command. Table 8.2 shows the protocol specifications of lock signal.

Table 8.2 Lock Signal Specifications

MODESET “Lock port set” field	CRZ(TPS4) “frequency mode” field	LOCK pin
0	2, 3, 4	Logic H
	other than above values	Logic L
1 (default)	2, 3	Logic H
	other than above values	Logic L
2	3	Logic H
	other than above value	Logic L
3	3,4	Logic H
	other than above values	Logic L

8.3 EPPS Signal

TBD

8.4 Backup Power (VBK)

TBD

9 State Transition

It is able to confirm the state transition by "frequency mode" field in CRZ (TPS4) sentence. See the protocol specifications about this sentence.

10 Environmental Specification

Table 10.1 Environmental Specification

Items		Specification	Unit	Notes
Operating temperature	GF-8701	-40 to +85	°C	
	GF-8702	-40 to +85	°C	
	GF-8703	-40 to +85	°C	
Storage temperature		-40 to +85	°C	
Operating humidity		85 (MAX)	%R.H	Ta= 60 °C, No condensation

11 RoHS, CE Marking, Frame retardant

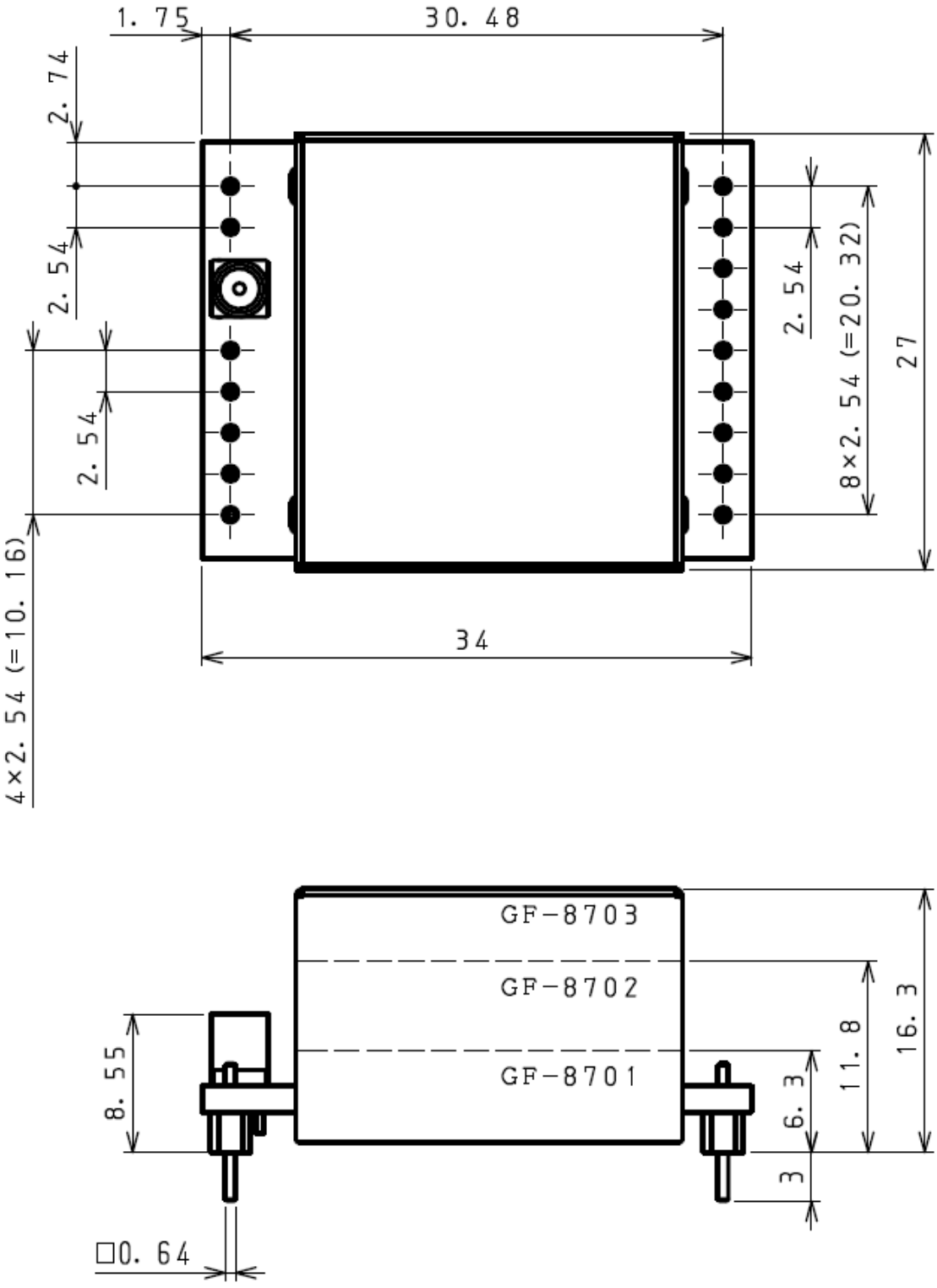
TBD

12 Reliability Test Item

#	Test Item	Conditions
1	High temperature high humidity bias life	1000 hours, T_A = 85℃, RH =85%
2	High temperature high humidity storage life	1000 hours, T_A = 85℃, RH =85%
3	Low temperature operating life	500 hours, T_A = -40℃
4	Low temperature storage life	500 hours, T_A = -40℃
5	Drop Test	With packing, 50cm natural drop
6	Vibration Test	The each three direction (x,y,z), 10 to 55Hz 4.7G (46m/s^2) 30 minutes (Not operating).

13 Mechanical Specification

13.1 Outline drawing



Note:
Tolerance ±0.2mm

14 Packaging

TBD

15 Special Attention

15.1 Precaution for users

(1) The GNSS receiver receives very weak signals from satellites. If you use the antenna that has not sufficient band limitation, you may not be able to obtain stable signals due to interferences from TV, mobile phones, etc. We recommend using antenna that has a filter in the preamplifier.

(2) Antenna should be installed in perpendicular to the ground outside with good open sky above 5 degree angular without any obstacles. GNSS signals are reflected by buildings, trees and ground etc and reach the antenna. Since these reflected signals cause errors, try to avoid the places where these reflections are expected.

(3) Radio signals from radiotelephones or transmitter antenna may come in to GNSS antenna and cause bad effects. Pay careful attention to the installation site avoiding the direction of radio beams.

(4) Noises from electronic devices may cause bad effects through antennas. Try to avoid using this product near such electronic noise sources.

(5) In consideration of above various reasons, we recommend to make a site investigation to check satellite acquisition status prior to fixing the antenna location.

(6) Do not do hot swap with power line connector or signal line connector.

(7)Try to avoid the wind if you use fan near the unit since the wind may cause error.

(8)Improper heat dissipation may increase the device temperature beyond the upper limit of the specifications, thus resulting in performance degradation or failure. Install the device, allowing sufficient space around the device, with heat dissipation taken into consideration.

(9) Lightning may strike the GNSS antenna. Since this product does not have a lightning protection, we recommend inserting an arrester between the GNSS antenna and this product.

15.2 Electronic component

In our GNSS receiver, we use chip resisters, capacitors, memories,
and TCXO's supplied from multiple manufacturers. Even in the same production lot, the GNSS receiver may incorporate these electronic components supplied from different manufacturers.

15.3 Precautions at Mounting

(1) This product contains semi-conductor inside. While handling this, be careful about the static electrical charge (less than 100 v). To avoid it, use conductive mat, ground wristband, anti-static shoes, ionizer, etc. as may be necessary.

(2) Try to avoid mechanical shock and vibration. Try not to drop this product.

15.4 Precautions on Intellectual Property Rights

(1) Since this document includes our copyrights and know-how, do not use it for any purpose other than the intended use of this product. Do not make any copies of this document and disclose it to any third parties without our prior consent.

(2) Except the use of this product itself, the sale and its disposal, the sale of this product to you does not grant explicitly or implicitly the right of use or implement any Intellectual Property rights or any other rights contained in this product to your company.

15.5 Restrictions of Export for Security

(1) Based on international regulations, the export of this product is prohibited when end users or end applications are involved or suspicious to be involved in development, manufacturing or usage of weapons of mass destruction.

(2) If you intend to export this product, please contact us beforehand.
Contact: 2-20 Nishinomiya-hama, Nishinomiya, Japan
Tel: +81-798-33-9588

15.6 Contact information

FURUNO ELECTRIC CO., LTD
2-20 Nishinomiya-Hama
Nishinomiya, Japan
Tel: +81-798-33-9588

FURUNO U.S.A., Inc.
GPS/OEM Timing Division
70 Engerman Avenue
Denton, MD 21629
Tel: +1 (410) 479-4420
Fax: +1 (410) 479-4429
gpssales@furuno.com

FURUNO DEUTSCHLAND GmbH
Konrad Zuse Platz 8 Munich 81829 Germany
Tel: +49 (89) 207-042-340
support@eRide.com