FURUNO

FURUNO GNSS Receiver

GT-87

Hardware Specifications

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FURUNO ELECTRIC CO., LTD.

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- Galileo(Europe)
- QZSS(Japan)
- SBAS(USA：WASS、Europe：EGNOS、Japan：MSAS)

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Revision History

Revision#	Revised description	Date
0	Initial Release	2013.05.17
1	Page 2: add Figure 3.1 Page 3: update chapter 4 Page 5-7: update chapter 6.1, 6.3, 6.4 and 6.5 Page 11: update Table 8.1	2013.05.31
2	Page 2: update Table 3.1 Page 4: update Table 5.1 Page 5: update Table 6.2 Page 9: update Table 6.7.1 Page 12: update Table 9.1 Page 12: add section 9.2 and 9.3 Page 13: adds notes in section 10.1 Page :14: update Figure 10.2.1 and Figure 10.2.2 Page 15: add chapter 11 Page 15: add chapter 12 Page 18: add chapter 13 Page 19: add chapter 14 Page 20: update chapter 16	2013.09.19
3	Page 3 update Figure .4.1 Page 4: update Table 5.1 Page 5: update Table 6.1 Page 6: update Table 6.2 and Figure 6.2 Page 8: update section 6.5.1 Page 8: update section 6.5.2 Page 9 update section 6.6 Page 11: update Table 8 Page 16: remove chapter 12 (Package) Page 19: update chapter 15	2014.09.29

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1. Outline

GT-87 is a stand alone, complete GNSS timing receiver module. It is designed to provide accurate timing pulse (PPS) to customers' various applications that are required to be synchronized to UTC time.
Main features are as follows.

- Supports GPS, GLONASS, SBAS, QZSS and Galileo(*1) with the latest *eRide*OPUS 7 monolithic GNSS receiver chip.
- Provides highly accurate PPS signal for various synchronization application with outputting PVT (Position, Velocity and Time) information through serial communication channel.
- Supports firmware update through serial communication channel.
- Fully integrated GNSS firmware executes acquisition, tracking, navigation, and data output for multiple constellations.
- Active Anti-jamming technology removes up to 8 CW jammers efficiently.
- Multi path mitigation technology maintains high accuracy even in the urban canyon.
- Works in both Autonomous mode and Assisted modes.
- GNSS high sensitivity enables to use at deep indoor environment.
- Both active and passive antenna usable.
- Low profile, small SMT package reducing foot print on PCB and assembly cost.

Notes:
(*1) For Galileo reception, firmware update is required.

2. GNSS General Specifications

Table 2.1 General Specifications

Item	Description		Notes
GNSS reception capability	GPS L1 C/A	12	
	SBAS L1C/A	2	
	GLONASS L1OF	10	
	Galileo E1B/E1C	8	(*1)
	QZSS L1C/A	2	
GNSS Concurrent reception	GPS, SBAS, GLONASS, Galileo and QZSS	34	(*1)
Environment robustness performance	Active Anti-jamming	8CW	
	Multipath Mitigation	●	
Serial data format	NMEA (Default)	●	Ver. 4.10, 38.4 kbps (*2)
	Binary	●	M12 binary protocol (*2)
Antenna	Active Antenna	●	
	Passive Antenna	●	
Operational Limits	Altitude	18,000 m	Compliant with the Wassenaar Arrangement Specifications
	Velocity	515 m/s	

Notes:
(*1) Firmware update required for enabling Galileo reception.
(*2) See Protocol Specifications for details.

3. GNSS General Performance

Table 3.1 General Performance

T_A=25°C, unless otherwise stated

Item	Description		Notes
TTFF	Hot Outdoor	<5 sec	These are specified with the measurement platform shown in Figure 3.1. Simulator output level is set to -130 dBm.
	Warm Outdoor	35 sec	
	Cold Outdoor	35 sec	
GPS Sensitivity (*1)	Tracking	-161 dBm	These are specified with the measurement platform shown in Figure 3.1.
	Hot Acquisition	-161 dBm	
	Cold Acquisition	-147 dBm	
	Reacquisition	-161 dBm	
GLONASS Sensitivity (*1)	Tracking	-157 dBm	
	Hot Acquisition	-157 dBm	
	Cold Acquisition	-143 dBm	
	Reacquisition	-157 dBm	
Position Accuracy	Horizontal Outdoor	2.5 m CEP	GPS only Open sky 24 hours with recommended antenna
		2.0 m CEP	GPS, GLONASS and SBAS Open sky 24 hours with recommended antenna
PPS Accuracy (*1)	1 Sigma	15 nano sec	Open sky, Static with recommended antenna

Δ2

Notes:
(*1) Update rate: 1 Hz.

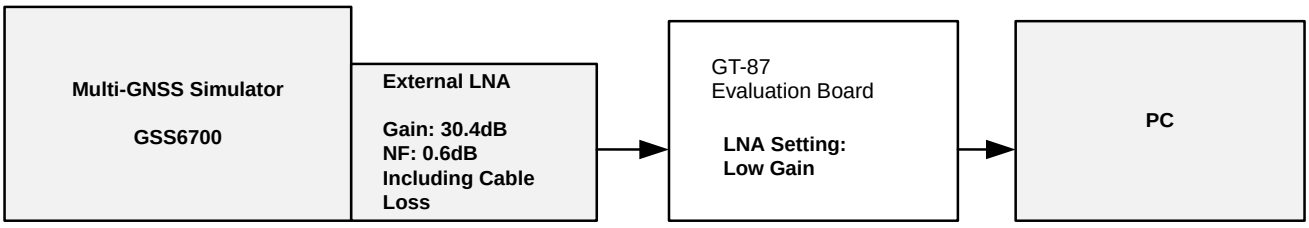


Figure 3.1 Measurement Platform

4. Function Overview

GT-87 is a stand alone, complete GNSS timing receiver module that can provide accurate PPS signal with GNSS PVT (Position, Velocity & Time) information through serial communication channel. The key device inside is *eRide*OPUS 7, the latest monolithic GNSS receiver chip that contains ARM9^{TM} processor for signal tracking and processing, high performance integrated LNA, PLL Synthesizer, Down-converter, ADC and DSP. GT-87 also contains Flash ROM for firmware and data storage, TCXO for reference clock, 32 kHz X'tal for RTC (Real time clock), L1 band SAW filter and power-on reset circuit. The block diagram is shown in Figure 4.1.

PPS pin provides accurate timing pulse which is synchronized to UTC(GPS) time system. The frequency of PPS signal is configurable by commands through serial communication channel (RXD1). Also GCLK pin provides clock output synchronized to PPS. The frequency of GCLK is configured by serial command from 4 kHz up to 40 MHz with 1 Hz step, and the rising edge of PPS pulse is synchronized to GCLK rising.

GT-87 has power-on reset function inside. It detects VCC input voltage, and sets internal power-on reset signal (POR_N) to logic L when the voltage is lower than power-on reset threshold voltage shown in Table 6.4.1. GT-87 also has external reset signal input, RST_N, which allows to force GT-87 reset by external control. RST_N and POR_N are wired-ORed to create internal reset signal for initializing whole module.

FLNA pin has a special function to configure LNA gain. In case this pin is connected to VCC, internal LNA is set to low gain mode. And in case of no connection (open), high gain mode is selected. So for active antenna, this pin should be connected to VCC, and for passive antenna open.

ANT_DET0/ANT_DET1 pins are used to feed the status of active antenna connection to ARM^{TM} subsystem from the antenna current detection circuit placed outside of GT-87. These signals can show three (3) states of antenna connection, that are normal, open (low current) and short (high current). For details, please refer "FURUNO 86/87 module products series user's design guide (SE13-900-001)".

Reserved pins have pull up or pull down registers inside adequately, so please do not connect anything.

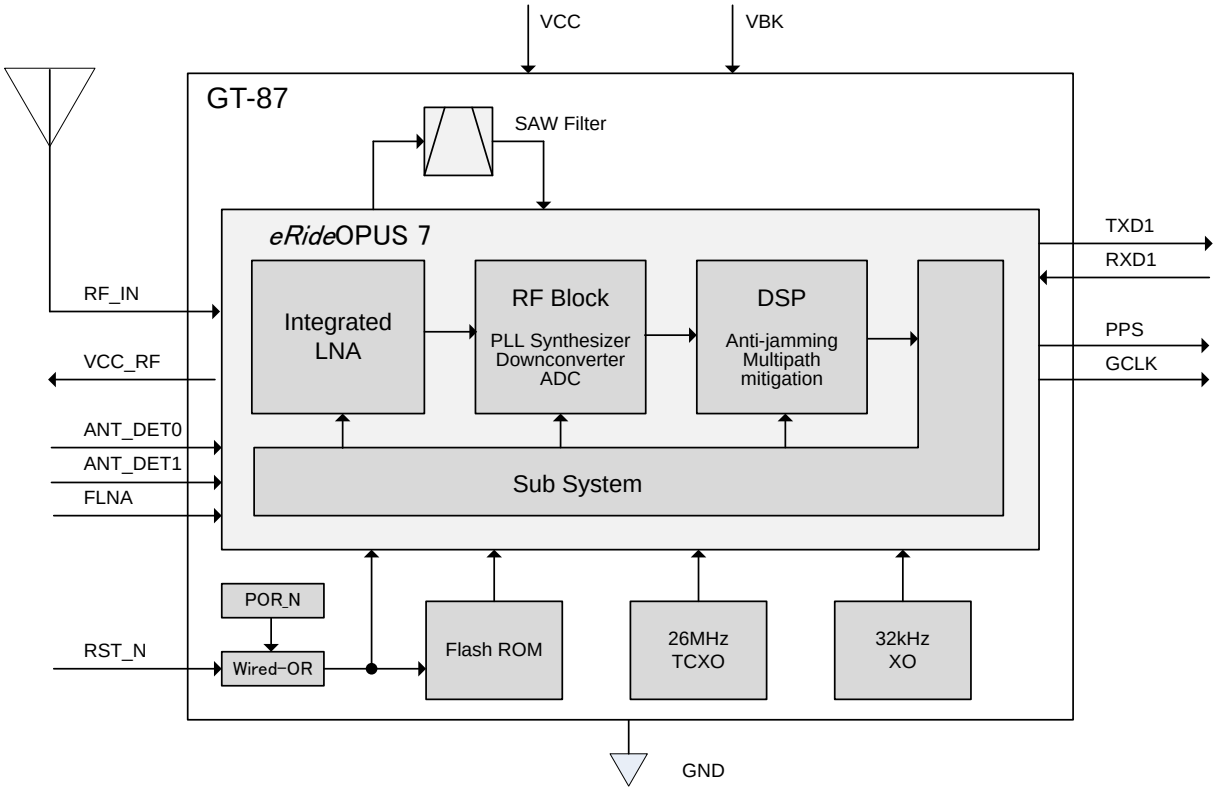


Figure 4.1 Block Diagram

5. I/O Signal Description

Table 5.1 I/O Signal Description

#	Pin Name	Type	PU/PD(*1)	Description
1	RESERVED	-	-	Do not connect anything
2	FLNA	Digital input	Pull-down	LNA gain select pin Logic L(leave open) : High gain Logic H(connect to VCC) : Low gain
3	PPS	Digital output	Pull-down	Pulse per second output pin Do not pull up externally (*2)
4	RESERVED	-	-	Do not connect anything
5	ANT_DET1	Digital input	Pull-up	Antenna detection input pins(*3)
6	ANT_DET0	Digital input	Pull-up	
7	RESERVED	-	-	Do not connect anything
Δ3 8	RST_N	Digital input/output	Pull-up	External reset signal input pin Logic L : Reset Logic H(Open) (*4) : Normal Operation
9	VCC_RF	Power output	-	Power supply output pin for active antenna
10	GND	-	-	Ground
11	RF_IN	Analog input	-	GNSS signal input pin
12	GND	-	-	Ground
13	GND	-	-	Ground
14	RESERVED	-	-	Do not connect anything.
15	GCLK	Digital output	Pull-down	Clock output pin Do not pull up externally (*2)
16	RESERVED	-	-	Do not connect anything.
17	RESERVED	-	-	Do not connect anything.
18	RESERVED	-	-	Do not connect anything.
19	RESERVED	-	-	Do not connect anything.
20	TXD1	Digital output	-	UART1 transmission output pin
21	RXD1	Digital input	Pull-up	UART1 reception input pin
Δ2 Δ3 22	VBK	Power Input	-	Backup power supply input pin Do not connect if battery backup function is not used
23	VCC	Power Input	-	Main power supply input pin
24	GND	-	-	Ground

Notes:

(*1) Pull-up and pull-down register values are shown in Table 6.3.

(*2) These pins have pull-down registers inside to ensure power-on configuration, so it is prohibited to connect any pull-up register at the outside of the module.

(*3) For details, see FURUNO GPS/GNSS Receiver 86/87 series User's Design Guide. (SE13-900-001)

(*4) RST_N is wired-ORed with internal power-on reset (POR_N) signal, so please drive with open-drain or open-collector device.

6. Electrical Characteristics

6.1. Absolute Maximum Rating

The lists of absolute maximum ratings are specified over Operating Temperature shown in Table 7.1. Stresses beyond those listed under those range may cause permanent damage to module.

Table 6.1 Absolute Maximum Rating

Items	Symbol	Min.	Max.	Unit	Notes
Supply voltage	V_{CC}	-0.3	4.0	V	
Backup supply voltage	V_{BK}	-0.3	4.0	V	
Digital input (DI) voltage	-	-0.3	4.0	V	
Digital output (DO) current	-	-	±7	mA	
VCC_RF output current	I_{CC_RF}		150	mA	
RF_IN input power (High Gain mode)	P_{RFINH_ABS}		-20	dBm	at 1575.42MHz & 1602MHz
			1	dBm	at 900MHz
			1	dBm	at 1800MHz
RF_IN Input power (Low Gain mode)	P_{RFINL_ABS}		-5	dBm	at 1575.42MHz & 1602MHz
			0	dBm	at 900MHz
			-1	dBm	at 1800MHz

Δ3

6.2. Power Supply

Table 6.2 Power Supply Characteristics

T_A=25°C, unless otherwise stated

	Items	Symbol	Min.	Typ.	Max.	Unit	Notes
	Supply voltage to pin VCC	V_{CC}	3.0	3.3	3.6	V	
	Backup supply to pin VBK	V_{BK}	1.4	-	3.6	V	
	Rising slew rate of VCC	V_{CC_SR}	-	-	$3.6x10^4$	V/s	See Figure 6.2.
Δ3	Rising slew rate of VBK	V_{BK_SR}	3.6	-	$3.6x10^4$	V/s	See Figure 6.2.
	Output voltage from pin VCC_RF	V_{CC_RF}	V_{CC} -0.2	-	V_{CC}	V	$I_{CC\ RF}$=100mA
	VCC current consumption Low Gain Mode (FLNA: High)	I_{CCAL}	-	65.5	113.5	mA	Full search VCC =3.3V
		I_{CCTH}		58.5	-	mA	Tracking satellite outdoor @-130dBm signal level, VCC =3.3V
Δ2 Δ3	VCC current consumption High Gain mode (FLNA: Open)	I_{CCAH}	-	72	120	mA	Full search VCC =3.3V
		I_{CCTH}	-	65	-	mA	Tracking satellite outdoor @-130dBm signal level, VCC =3.3V
	VBK current consumption at back up	I_{BKN}	-	9	20	μA	V_{CC} =0V
	VBCK current consumption at normal operation	I_{BKB}	-	0.4	2	μA	V_{CC} =3.3V

Δ2 Δ3

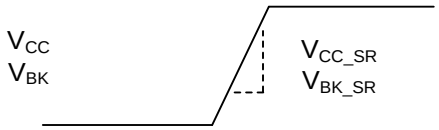


Figure 6.2 VCC/ VBK Rise Time

6.3. Interface Signals

Table 6.3 Interface Signals Specifications

T_A=25°C, unless otherwise stated

Items	Symbol	Min	Typ	Max	Unit	Notes
Logic L input voltage	V_{IL}	-	-	0.8	V	
Logic H input voltage	V_{IH}	2.0	-	-	V	
Hysteresis voltage	V_{HST}	0.31	-	-	V	
Logic L output voltage	V_{OL}	-	-	0.4	V	$\|I_{OL}\|$ = 2 mA
Logic H output voltage	V_{OH}	2.4	-	-	V	$\|L_{OH}\|$ = 2 mA
Equivalent pull-up resistor	R_{PU}	29	41	62	kΩ	
Equivalent pull-down resistor	R_{PD}	30	44	72	kΩ	

6.4. Reset

6.4.1. Internal Power-on Reset

GT-87 contains internal power-on reset circuit which detects VCC voltage and creates POR_N (power-on reset) signal for initializing module.

Table 6.4.1 shows the threshold voltages to detect and create POR_N signal.

Table 6.4.1 Power-on Reset Voltage

T_A=25°C, unless otherwise stated

Items	Symbol	Min	Typ	Max	Unit	Notes
Power On Reset Threshold voltage (rising)	V_{RTH_POR}	-	-	3.0	V	VCC rising
Power On Reset Threshold voltage (falling)	V_{FTH_POR}	2.70	-	-	V	VCC falling

6.4.2. External Reset

In most cases, it is not required to drive external reset input (RST_N) pin. However, if it is needed to force GT-87 being in reset state externally for e.g. synchronizing reset state with application circuitry, RST_N can be used for this purpose.

RST_N should be driven by open-drain or open-collector device for avoiding any collision with internal power-on reset driver.

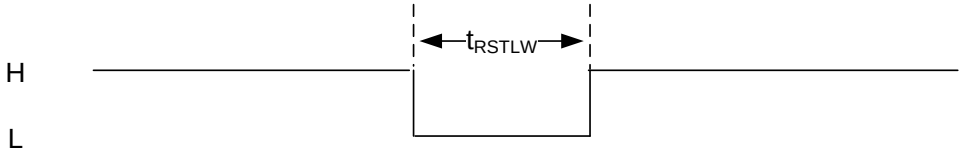


Figure 6.4.2. Reset Sequence

Table 6.4.2. Reset Sequence

Items	Symbol	Min	Max	Unit	Notes
RST_N pulse width	t_{RSTLW}	300	-	ms	

6.5. UART Wake-up Timing after Reset

6.5.1. Without External Reset

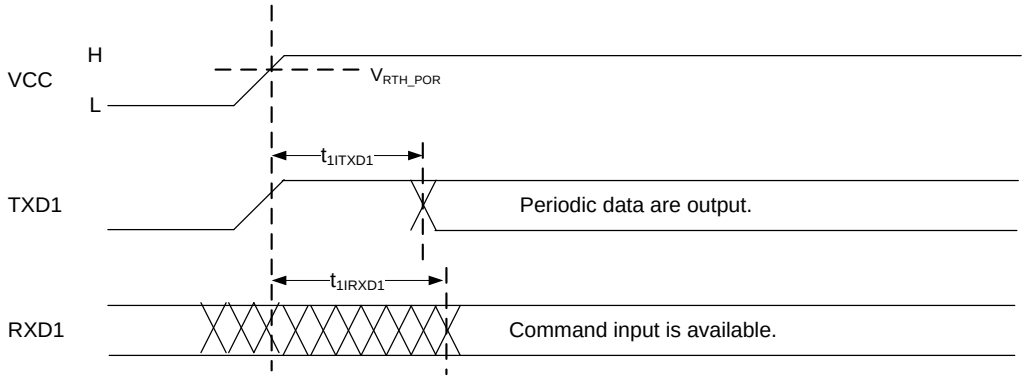


Figure 6.5.1 UART Wake-up Timing after V_{RTH_POR}

Δ3

Table 6.5.1 UART Wake-up Timing after V_{RTH_POR}

Items	Symbol	Min	Typ	Max	Unit	Notes
Time delay until periodic data are output after V_{CC} reaches V_{RTH_POR}	t_{1XTXD}	-	3.3	6	sec	
Time delay until the command input is available after V_{CC} reaches V_{RTH_POR}	t_{1XRXD}	-	3.3	6	sec	

6.5.2. With External Reset

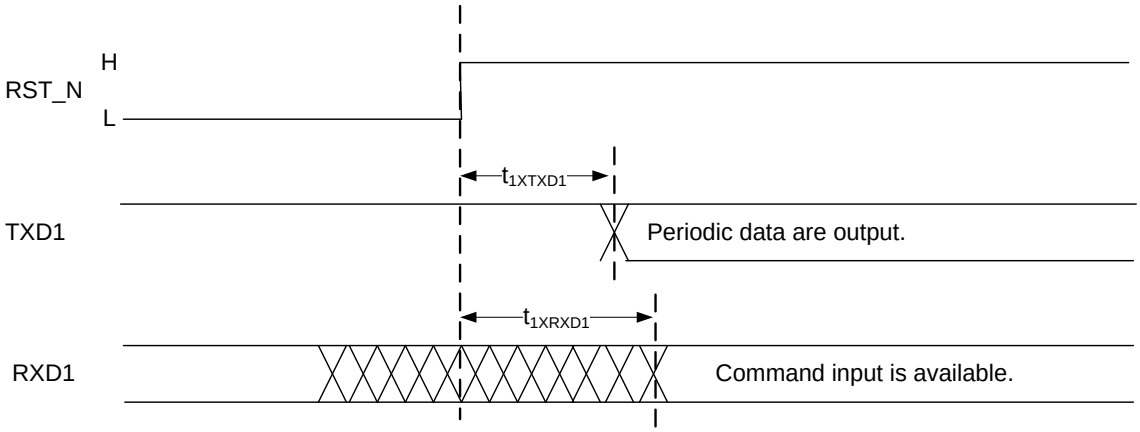


Figure 6.5.1 UART Wake-up Timing after RST_N

Δ3

Table 6.5.1 UART Wake-up Timing after RST_N

Items	Symbol	Min	Typ	Max	Unit	Notes
Time delay until periodic data are output after RST_N sets to H	t_{1XTXD}	-	3.1	6	sec	
Time delay until the command input is available after RST_N sets to H	t_{1XRXD}	-	3.1	6	sec	

6.6. Baud Rate Setting

Δ3 The UART inside GT-87 can handle various baud rate serial data shown in Table 6.6.
The baud rate clock is created from 71.5 MHz system clock, hence it has some deviation errors against ideal baud rate clock as shown in Table 6.6.

Table 6.6 Baud Rate vs Deviation Error

Baud rate [bps]	Deviation error [%]
4800	0.00
9600	0.11
19200	0.11
38400	0.32
57600	0.54
115200	0.54
230400	2.08

6.7. Recommended GNSS Antenna

6.7.1. Active Antenna

Table 6.7.1 Recommended Active Antenna

Items	Min	Typ	Max	Unit	Notes
GPS center frequency	-	1575.42	-	MHz	2.046 MHz bandwidth
GLONASS center frequency	-	1602	-	MHz	9 MHz bandwidth
Antenna element gain	0	-	-	dBi	
Amplifier gain1(*1)	-	-	35 (*1)	dB	Including cable loss High Gain mode (FLNA: Open)
Amplifier gain2(*1)	15		50 (*1)	dB	Including cable loss Low Gain mode (FLNA: High)
Amplifier NF	-	-	1.5	dB	
Impedance	-	50	-	Ω	
VSWR	-	-	2	―	

Δ2 **Note:**
(*1) For best jammer resistance (and lower power consumption) use 10 dB lower gain than the max gain.

6.7.2. Passive Antenna

Table 6.7.2 Recommended Passive Antenna

Item	Min	Typ	Max	Unit	Notes
GPS center frequency	-	1575.42	-	MHz	2.046 MHz bandwidth
GLONASS center frequency	-	1602	-	MHz	9 MHz bandwidth
Antenna element gain	0	-	-	dBi	FLNA: Open
Impedance	-	50	-	Ω	
VSWR	-	-	2	―	

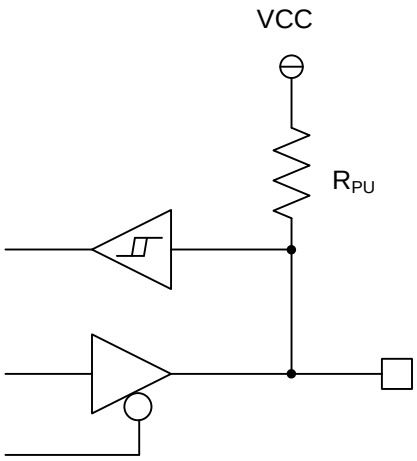
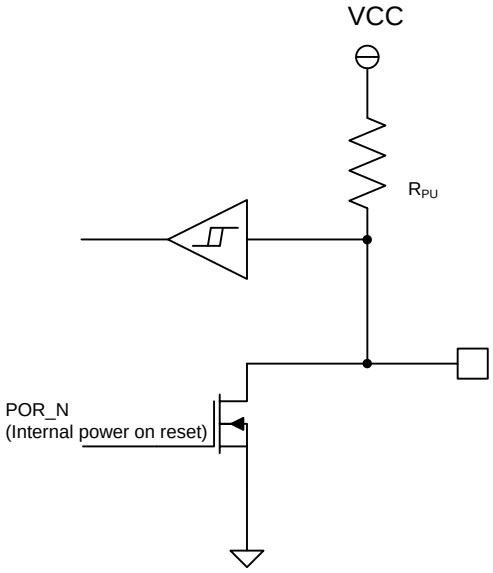
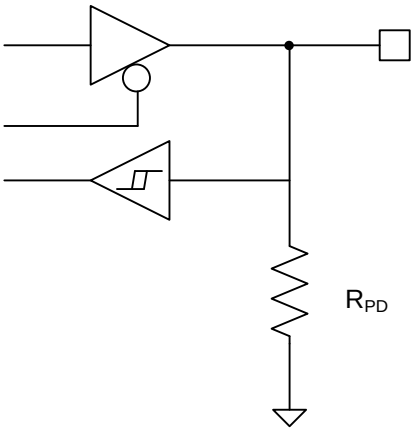
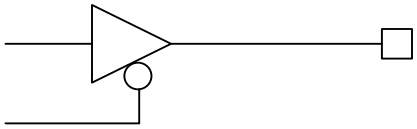
7. Environmental Specifications

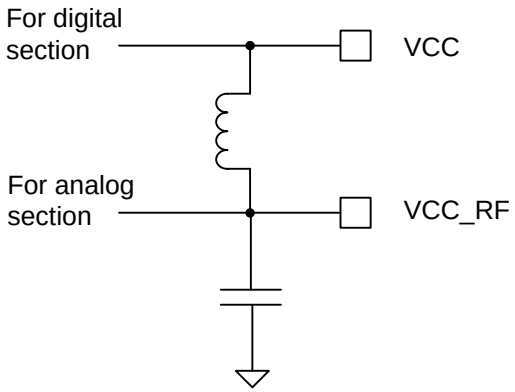
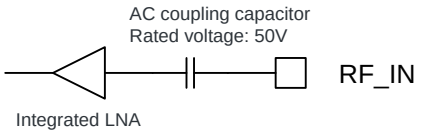
Table 7.1 Environmental Specifications

Item	Specification	Unit	Notes
Operating Temperature	-40 to +85	°C	
Storage Temperature	-40 to +85	°C	
Operating Humidity	85 (MAX)	%R.H	T_A= 60 °C, No condensation

8. Equivalent Circuit

Table 8.1 Equivalent Circuit

Pin Name	Equivalent Circuit
ANT_DET0, ANT_DET1, RXD1	
Δ3 RST_N	
FLNA, PPS,GCLK	
TXD1	

Pin Name	Equivalent Circuit
VCC_RF	
Δ3 RF_IN	

9. Mechanical Specifications

9.1. Package Dimension

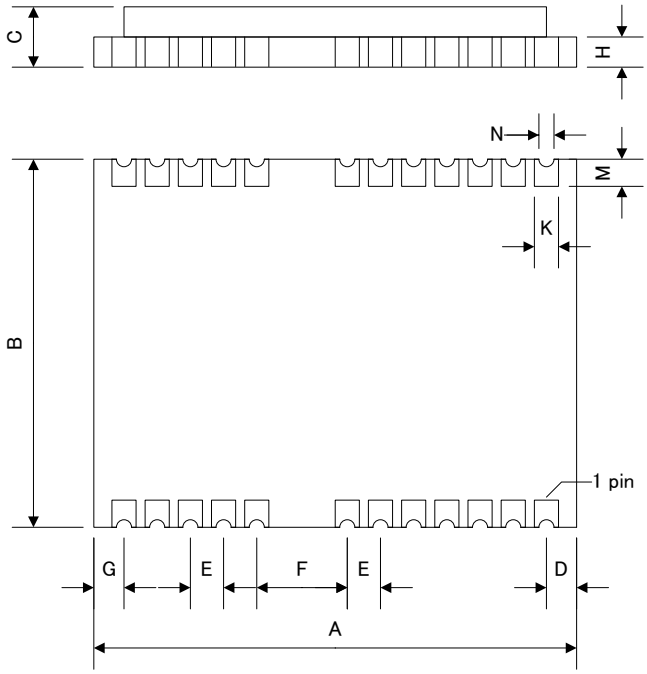


Figure 9.1 Package Dimension

Table 9.1 Package Dimension

	Min [mm]	Typ [mm]	Max [mm]
A	15.8	16.0	16.2
B	12.0	12.2	12.4
C	2.6	2.8	3.0
D	0.9	1.0	1.1
E	1.0	1.1	1.2
F	2.9	3.0	3.1
G	0.9	1.0	1.1
H	-	0.6	-
K	0.7	0.8	0.9
M	0.8	0.9	1.0
Δ2 N	0.4	0.5	0.6

Δ2 9.2. Electrode

Electrode Material: Cu
Metallic Finishing: Electroless gold flashing (Au: 0.3 μ and over Ni: 0.3 μ and over)

Δ2 9.3. Weight

1.01 g (Typ)

9.4. Pin Position List

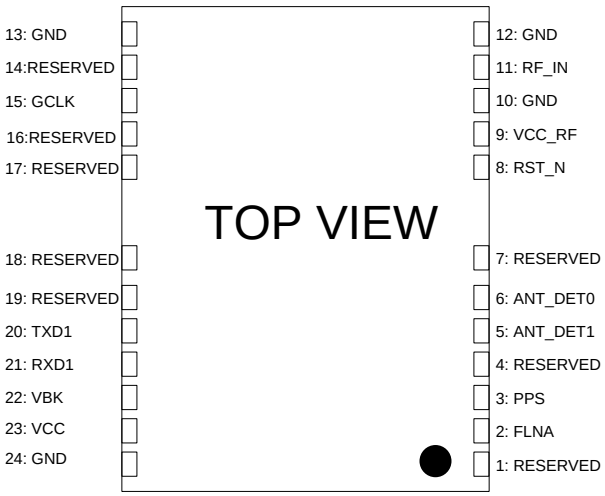
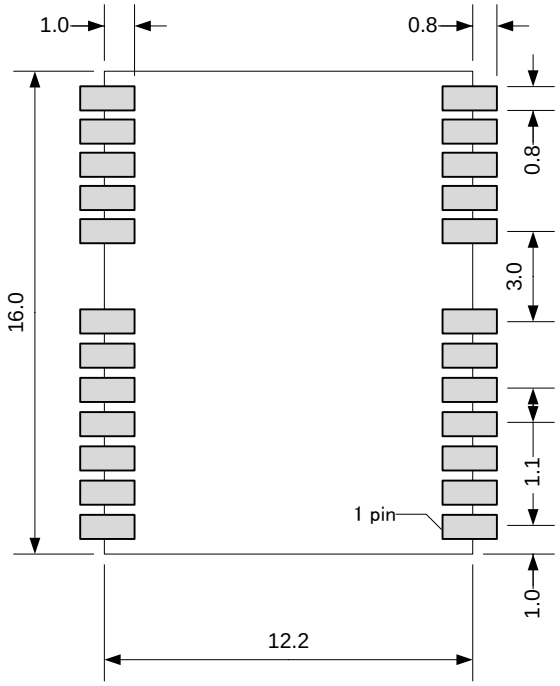


Figure 9.2 Pin Position List

10. Reference Design

10.1. Recommended Land Pattern



Unit: [mm]

Notes:

Δ2 At the bottom of the module, there are some signal lines and via holes. For avoiding any signal shortage, please do not put any signal line nor via hole at the part of the user's board where is facing to the bottom of the module.

Figure 10.1 Recommended Land Pattern

10.2. Example of Connection

10.2.1. With Active Antenna

Δ2

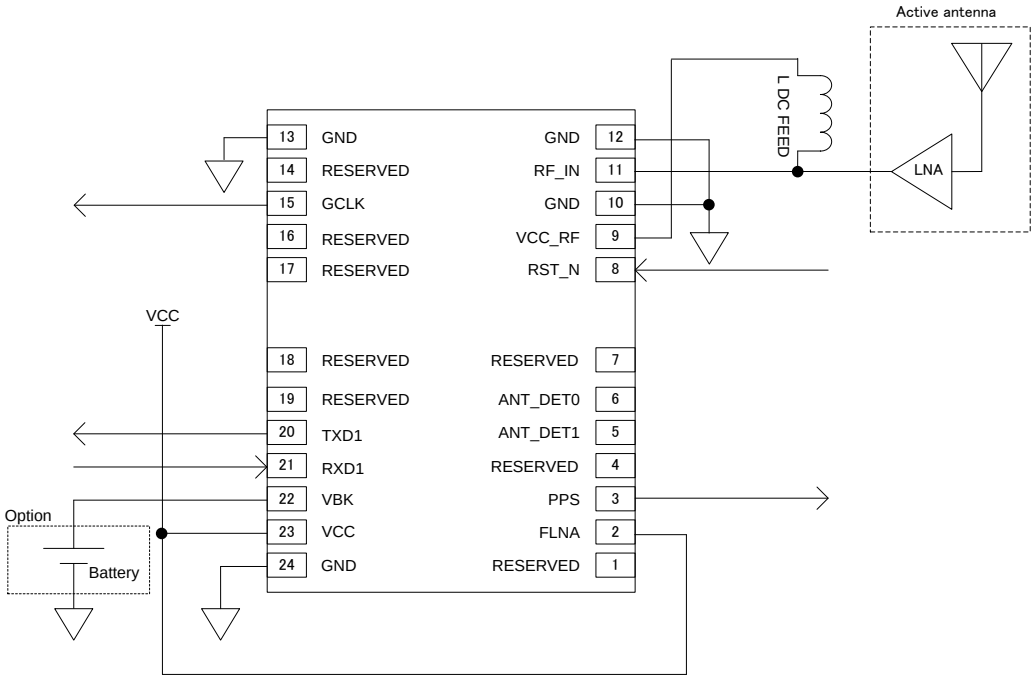


Figure 10.2 Example of Connection (with Active Antenna)

10.2.2. With Passive Antenna

Δ2

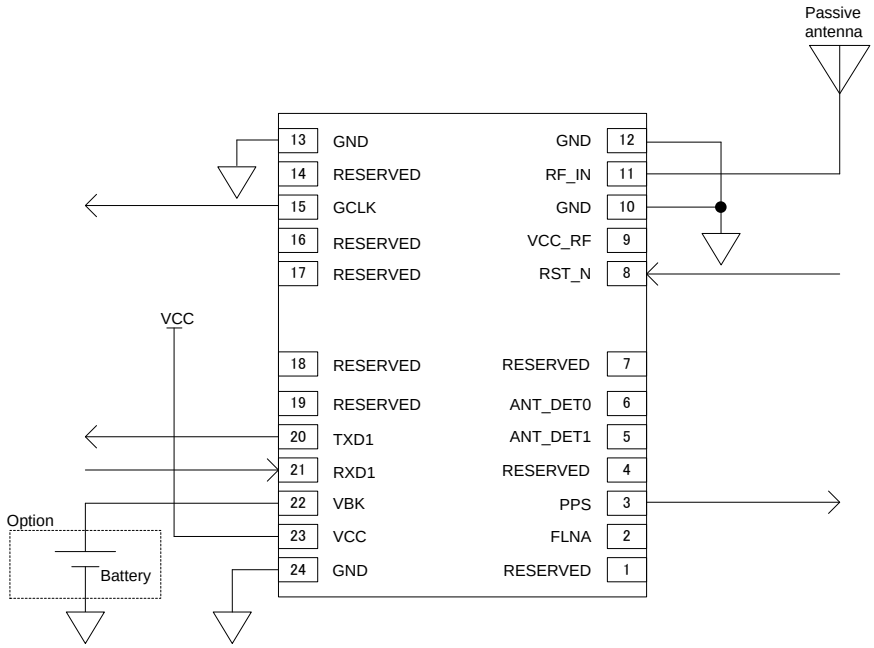
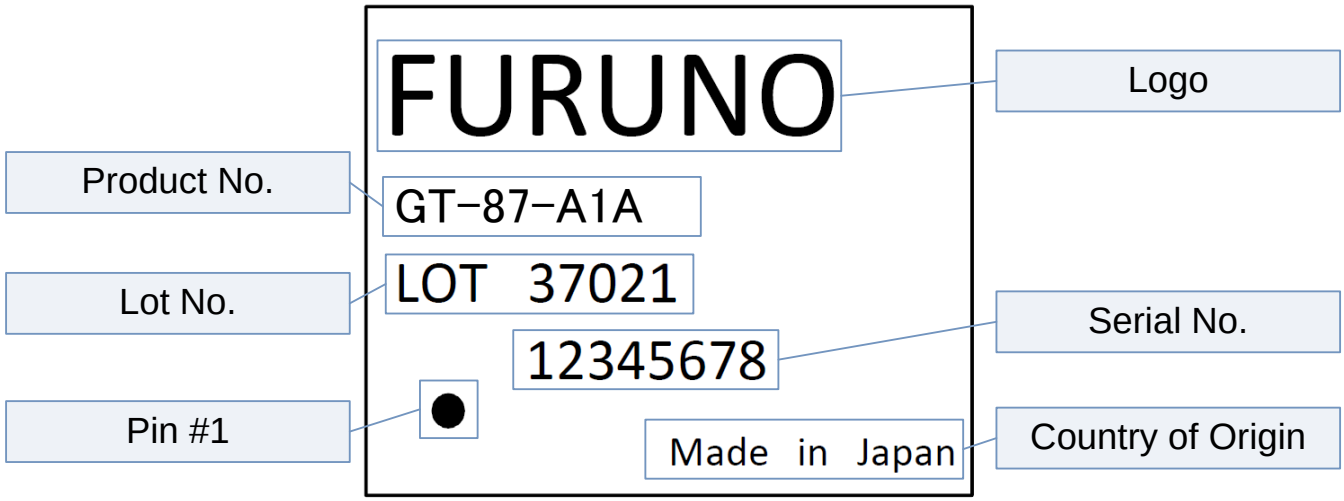
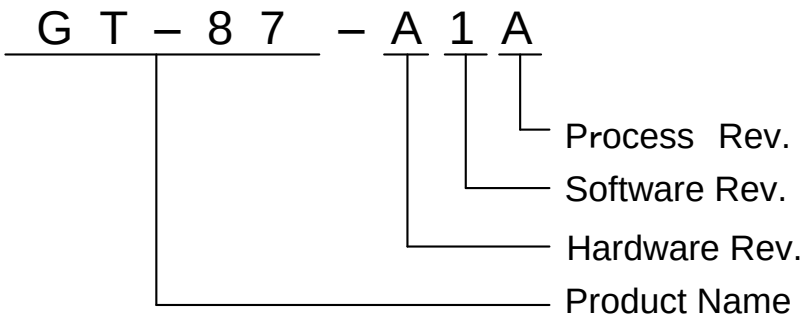


Figure 10.3 Example of Connection (with Passive Antenna)

Δ2

11. Marking





Δ2
Δ3

Δ2

12. Handling Precaution

The section especially describes the conditions and the requests when mounting the product.

Surface mount products like this may have a crack when thermal stress is applied during surface mount assembly after they absorb atmospheric moisture. Therefore, please observe the following precautions:

(1) This product contains semi-conductor inside. While handling this, be careful about the static electrical charge. To avoid it, use conductive mat, ground wristband, anti-static shoes, ionizer, etc. as may be necessary.
(2) Try to avoid mechanical shock and vibration. Try not to drop this product.
(3) When mounting this product, be aware of the location of the electrode.
(4) This product should not be washed.
(5) The reflow conditions are as shown in chapter 13. The reflow can be done twice at most.
(6) Surface mount products like this may have a crack when thermal stress is applied during surface mount assembly after they absorb atmospheric moisture. Therefore, please observe the following precautions:
   ① This moisture barrier bag may stored unopened 12 months at or below 30℃ /90%RH.
   ② After opening the moisture bag, this packages should be assembled within 1 week in the environment less than 30℃ /60%RH.
   ③ If, upon opening, the moisture indicator card in the bag shows humidity above 30% or the expiration date has passed, they may still be used with the addition of a bake of 24 hours at 125 ℃.
   Caution: If the packing material is likely to melt at 125 ℃, heat-proof tray or aluminum magazine etc. must be used for high temperature.
   ④ Expiration date: 12 months from the sealing date.

Δ3 (7) This module includes a crystal oscillator. It may not be able to maintain the characteristic under the vibrating condition, windy and cold conditions and noisy conditions. Please evaluate the module on ahead, if it may be used under the conditions.

Δ2

13. Solder Profile

13.1. Reflow Profile

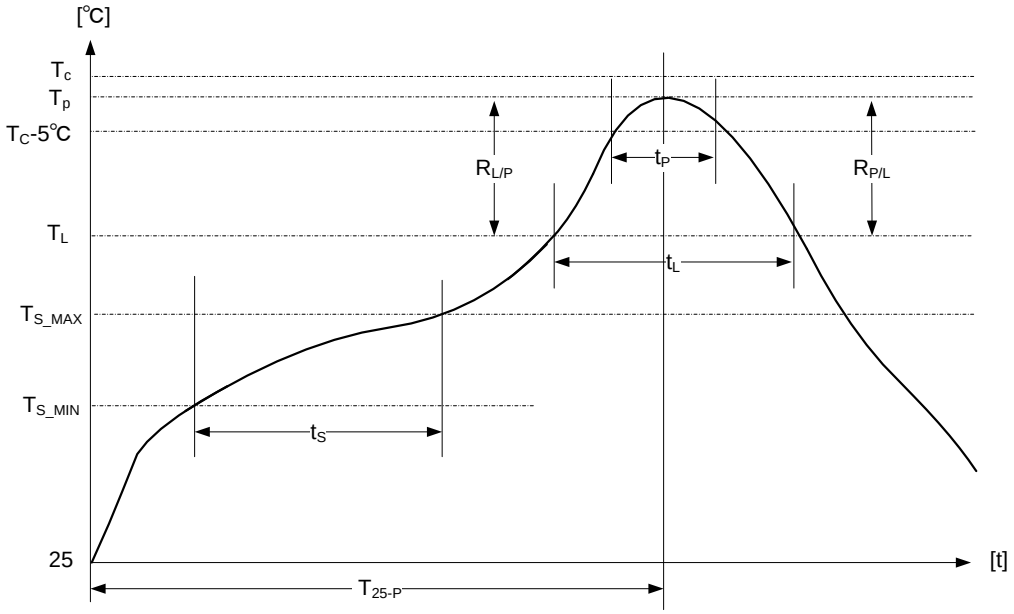


Figure 13.1 Condition of Reflow (Based on IPC/JEDEC J-SED-020D)

Table 13.1 Condition of Reflow (Pb-free)

Item	Symbol	Condition	Notes
Preheat/Soak Minimum Temperature	$T_{S\text{-}MIN}$	150℃	
Preheat/Soak Maximum Temperature	$T_{S\text{-}MAX}$	200℃	
Preheat/Soak Time from $T_{S\text{-}MIN}$ to $T_{S\text{-}MAX}$	t_S	60 to 120 sec	
Ramp-up rate T_L to T_P	$R_{L/P}$	3℃/sec (Max)	
Liquidous Temperature	T_L	217 to 220℃	
Time maintained above TL	t_L	60 to150 sec	
Specified classification temperature	T_C	245℃	
Time within 5 ℃ of TC	t_P	30 sec	Tolerance for tp is defined as a user maximum
Ramp-down rate T_L to T_P	$R_{P/L}$	6℃/sec (Max)	
Time 25 ℃ to peak temperature	$T_{25\text{-}P}$	8 min (Max)	

Notes:
- Please reflow according to Figure 13.1 and Table 13.1.
- Recommended temperature reflow profile pattern is lead free.
- Recommended atmosphere in chamber is Nitrogen.
- Oxygen density level is less than 1500 ppm.
- Profile temperature should be measured on top of the shielding case.
- Package condition except IPC/JEDEC J-STD-020D needs pre-baking.
- If customer should change to reflow profile from what we recommend due to temperature condition inside of reflow chamber. Please inquire us for impact on the following items.
  - ・Soldering of module pad on customer's board and our module
  - ・Solder re-melting of components mounted on our module

Table 13.2 shows the moisture sensitivity level and number of reflow for assembly at user side.

Table 13.2 Moisture Sensitivity Level, Number of Reflow for Assembly at User Side

Item	Condition
Moisture sensitivity level	3
Number of reflow for assembly at user side	2

13.2. Precaution about Partial Heating with the Way except Reflow

If the internal temperature when the product is heated partially with, for example, like a soldering iron, hot air and light beam welder exceeds 215 degree, the internal wiring may be disconnected by thermal stress.

14. Special Instruction

14.1. Electronic Component

Components in GT-87 module such as chip resisters, capacitors, memories and TCXO's are planned to be purchased from multiple manufacturers/vendors according to FURUNO's procurement policy. So it is possible that multiple components from multiple manufacturers/vendors could be used even in the same production lot.

14.2. ESD Damage

GT-87 module can be damaged by ESD. FURUNO recommends that all modules should be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

14.3. RoHS

GT-87 complies with RoHS directives.

15. Reference Documents

Δ3
- FURUNO 86/87 module Package Specifications (Document No. SE13-600-024)
- FURUNO 86/87 module products series reliability test (Document No. SE13-600-002)
- FURUNO GPS/GNSS Receiver 86/87 series User's Design Guide. (Document No. SE13-900-001)